



Layout : Q87/B85H3-AM co-lay
Schematic: Q87 only
Rev:1.0

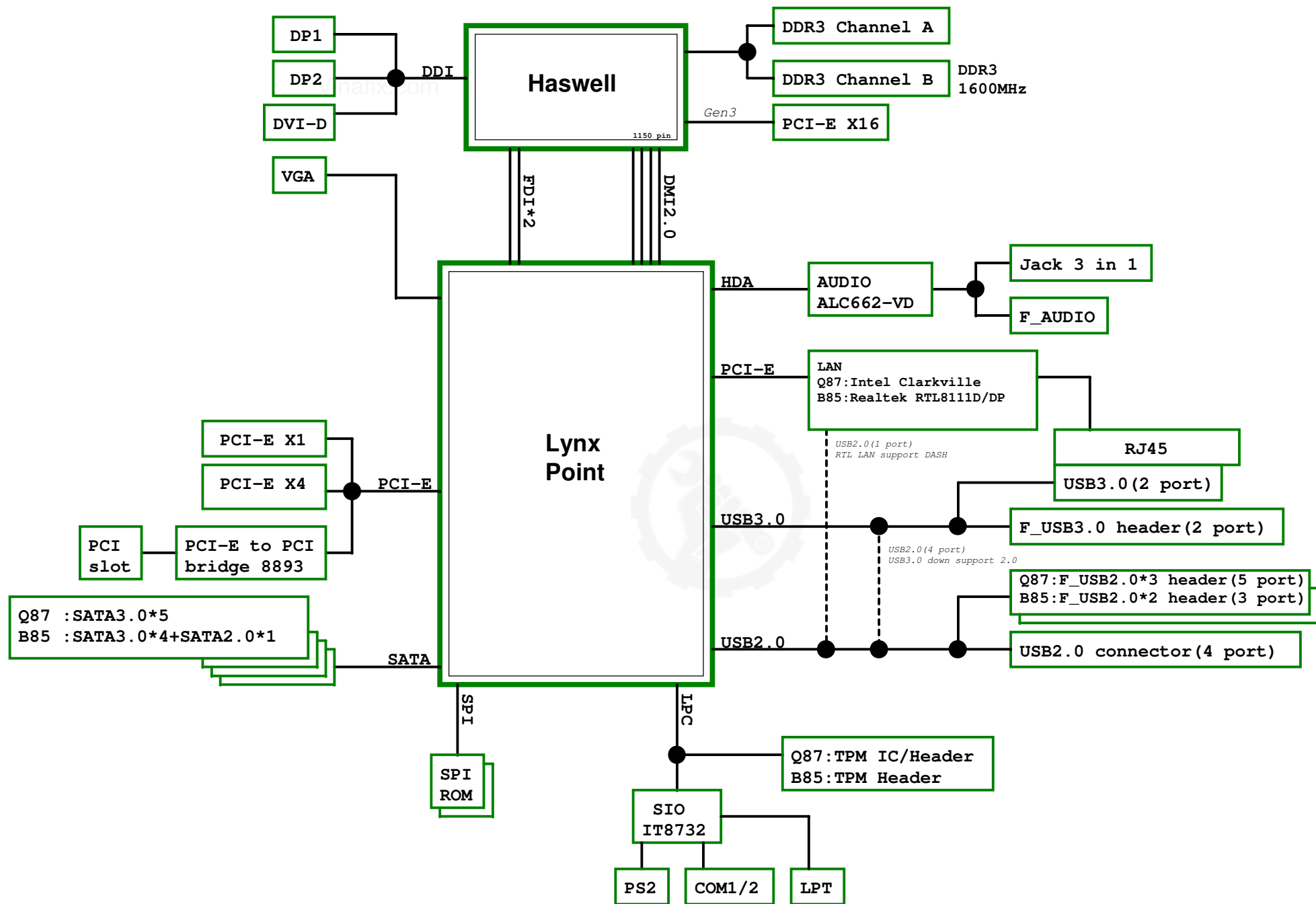
ECS
CONFIDENTIAL

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REVISION HISTORY:

Rev	Date	Notes
27		ECIO-IT8732
28		FAN/PS2/Buzzer/F_Panel
29		LPT/COM/TPM
30		LAN Intel & Realtek
31		LAN+USB3.0 Connector
32		AUDIO-ALC662_VD
33		AUDIO-CONN & Header
34		XDP-CPU/PCH
35		DC/DC VDIMM/DDR_VTT/5VDUAL
36		DC/DC PCH_1.5V/PCH,ME_1.05V
37		DC/DC ATX_3VSB/3VDUAL
38		DC/DC Vcore /Gate driver
39		DC/DC VCC3 & VCC & ATX12P
40		PWR Delivery
41		PWR Sequence/RST Diagram
42		CLK Distribution



PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO13	3VSB	LPC_PME	GPI
GPIO24	3VSB	USB_5VDUAL control (reserve)	GPO
GPIO72	3VSB	USB_5VDUAL control	Native
GPIO45	3VSB	BIOS WP	Native
GPIO57	3VSB	BIOS WP	GPI
GPIO46	3VSB	WLAN_DIS_L	Native
GPIO61	3VSB	LPCPD_L	Native
GPIO27	ATX_3VSB	ILAN_WAKE_L	GPI
GPIO1	VCC3	OBR	GPI
GPIO6	VCC3	Thermal_SD	GPI
GPIO68	VCC3	TP_VGA	GPI
GPIO23	VCC3	HDPANEL_DETECT	Native
GPIO15	3VSB	PEX16_RST	GPO
DL, BIOS must be pro			
GPIO73	3VSB	case open(reserve)	PCIECLKRQ0#
GPIO14	3VSB	ME_Disable	Native
GPIO19	VCC3	BOOT device detect	GPI
GPIO51	VCC3	BOOT device detect	GPO

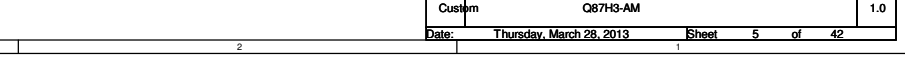
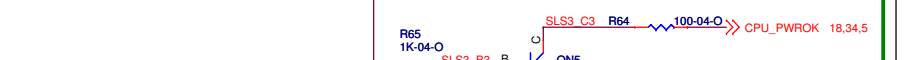
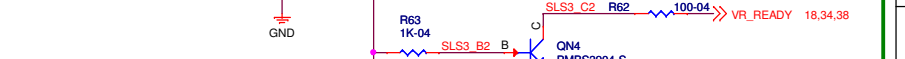
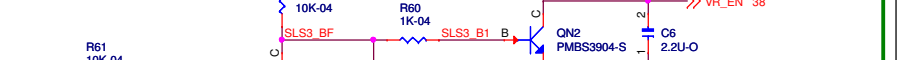
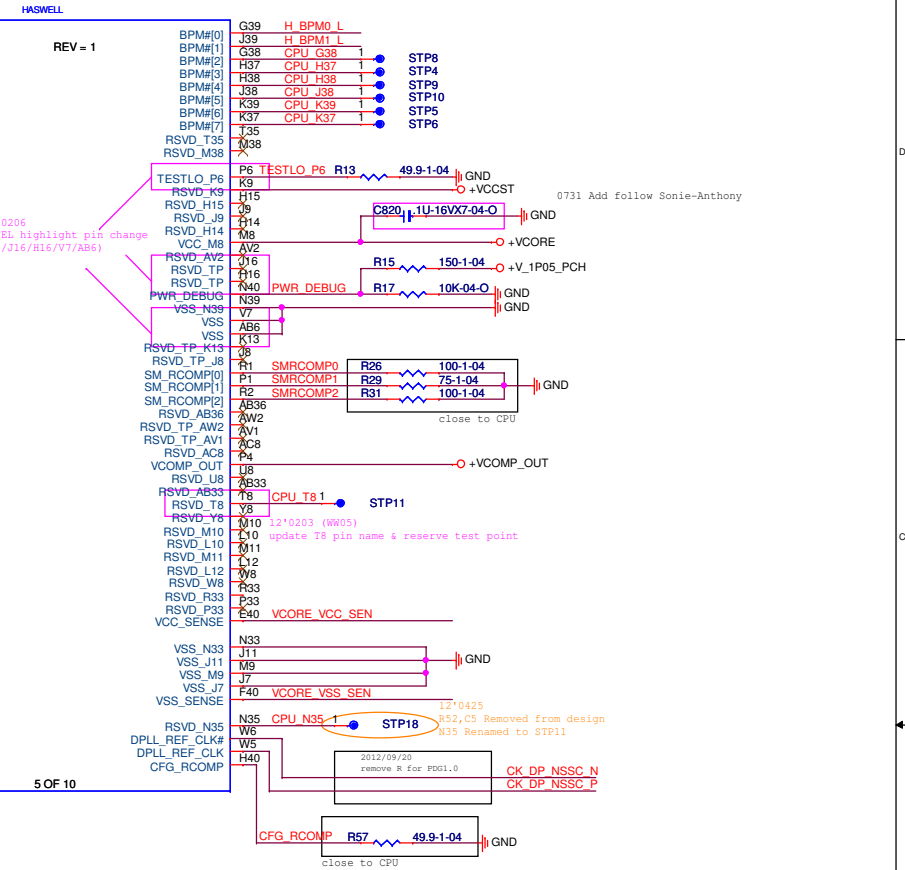
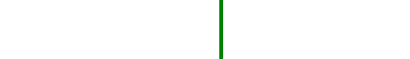
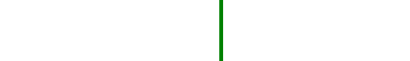
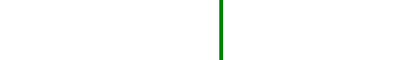
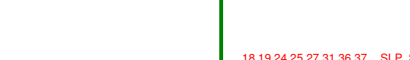
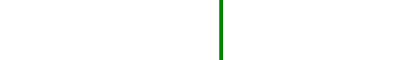
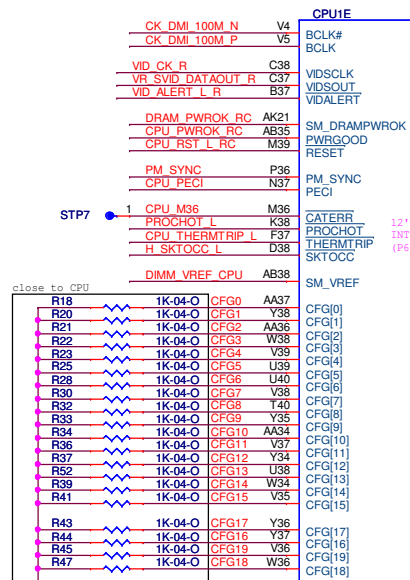
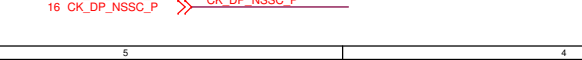
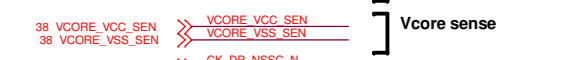
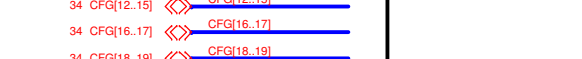
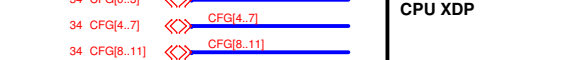
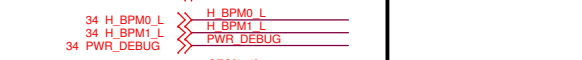
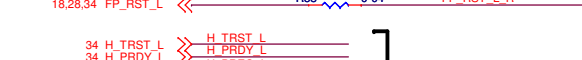
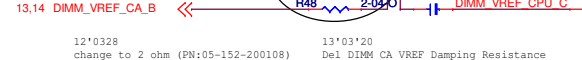
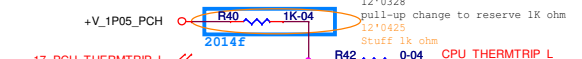
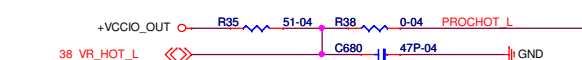
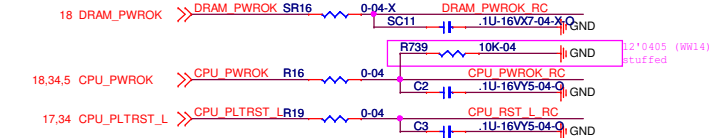
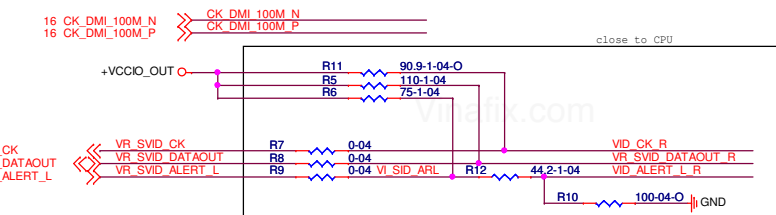
Interrupt mapping

Function	INT# port	PCle*1 port	Device
PCI Bridge	INTA#	port 1	IC IT8893
mini-PCIE	INTB#	port 2	LPT integrate
LAN	INTC#	port 3	Clarkville or RTL8111DP
PCIEX1	INTD#	port 4	LPT integrate
PCIEX4	INTA#/B#/C#/D#	port 5~8	LPT integrate
SATA	INTB#	NA	LPT integrate

SIO-GPIO function

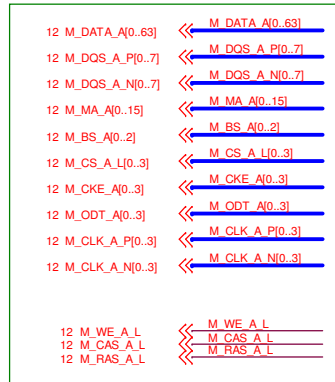
Pin Name	Power Well	Usage	Default Status
GP16	VCC3	Beep(reserve)	CIRRX2
GP36	3VSB	Thermal_SD	FAN_CTL3
These GPIO pins are kept by VCC in default but can be changed to be kept by 3VSB if EC side writes 1 to 2012h[bit 5].			
GP35	3VSB	LED0	FAN_TAC4
GP37	3VSB	LED1	FAN_TAC3
GP70	VCC3	TPM Onboard detect	GPIO
GP71	VCC3	BOM detect	GPIO
GP73	VCC3	BOM detect	GPIO
GP74	VCC3	BOM detect	GPIO
GP76	VCC3	Thermal_HD_Auto_Switch	GPIO
GP46	3VSB	Acer Header	GPIO
GP47	3VSB	Acer Header	GPIO
GP40	3VSB	5VDUAL Switch	3VSBSW

BIOS must be pro to Native 3VSBSW

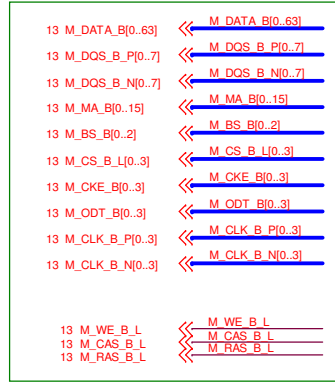


Power Down Sequencing Circuit

CPU-MISC		
Size	Document Number	Rev
Custom	Q87H3-AM	1.0
Date:	Thursday, March 28, 2013	Sheet 5 of 42



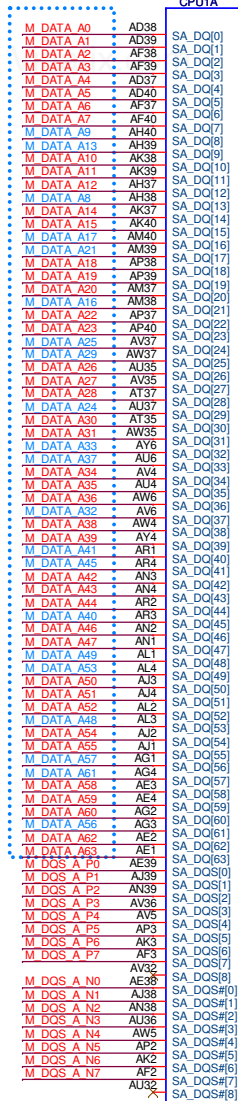
DDR3 CH.A



DDR3 CH.B

12,13,6 DDR3_DRAMRST_L << DDR3_DRAMRST_L

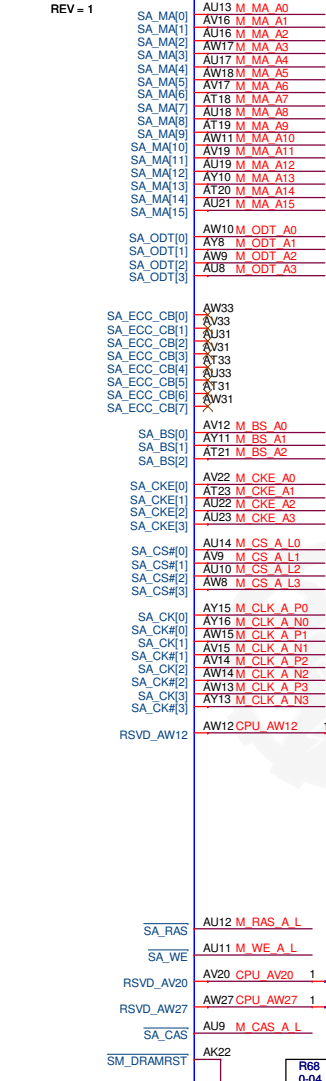
**Attention



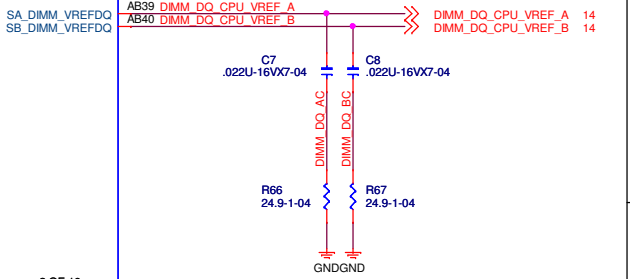
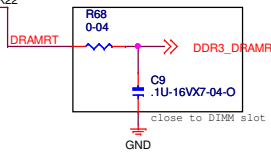
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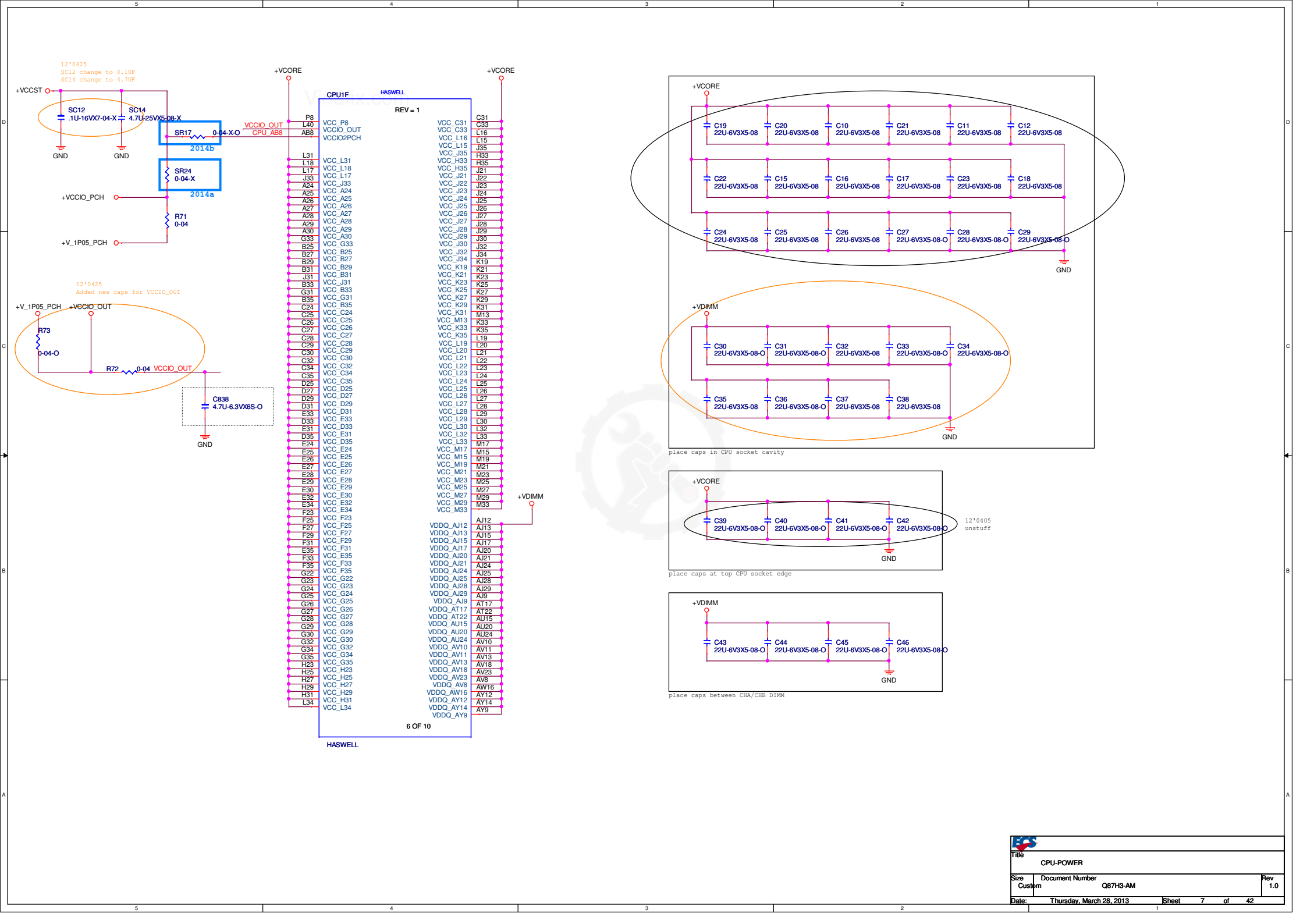
CPU1B HASWELL

REV = 1

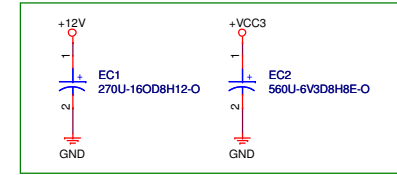
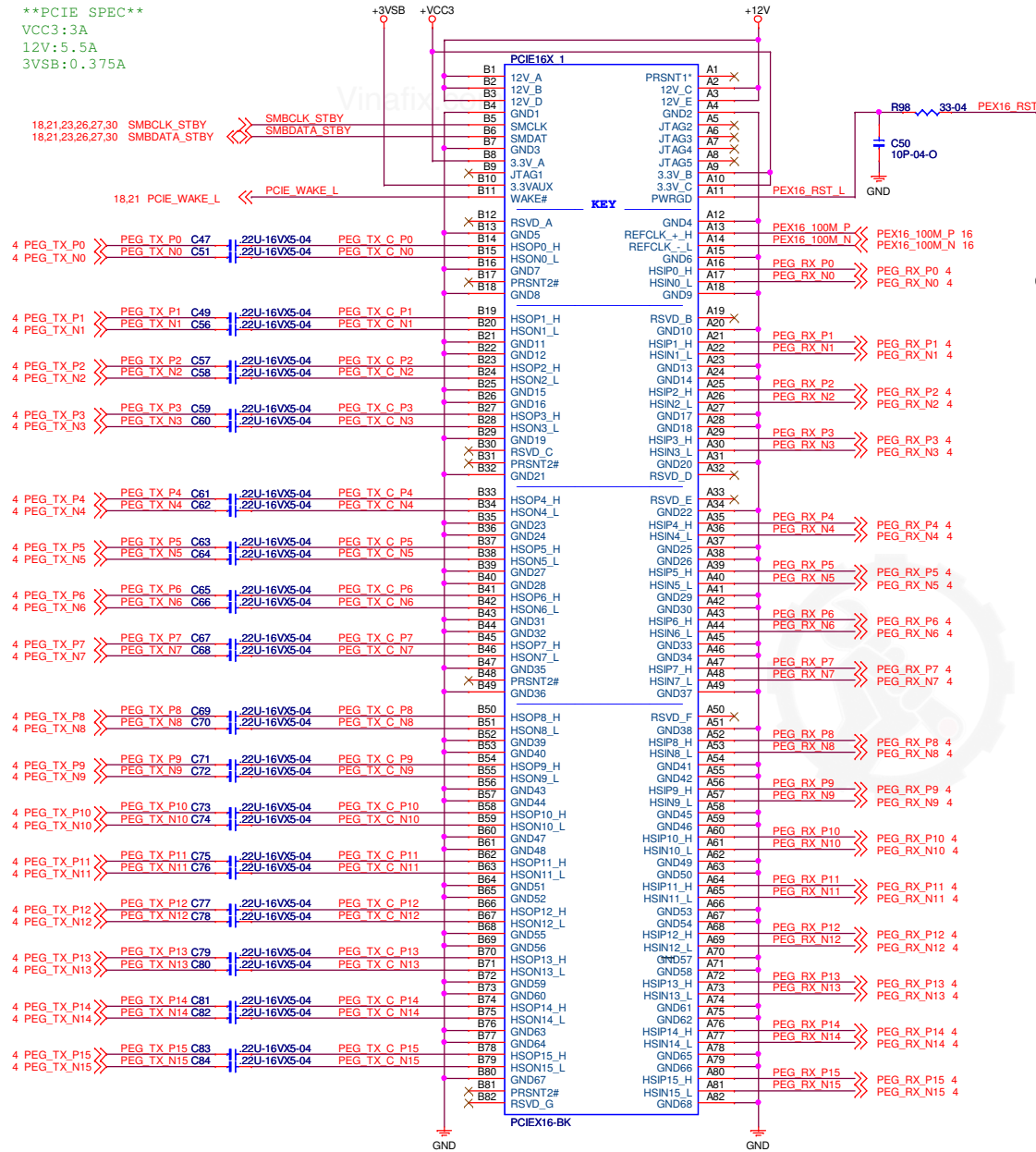


HASWELL

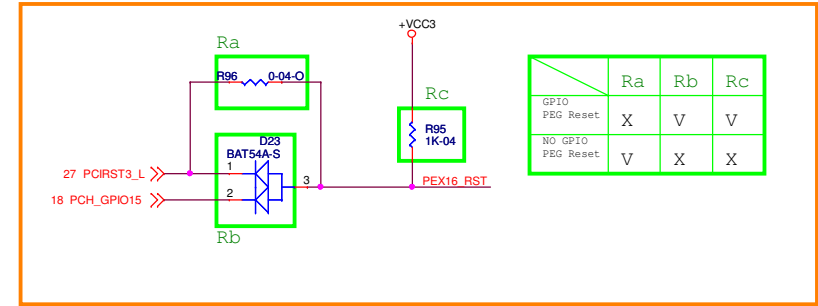
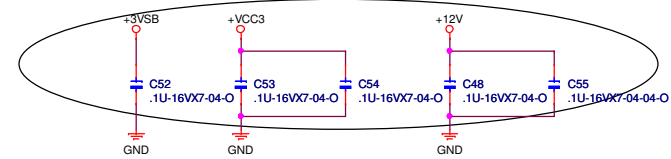




PCIE SPEC
VCC3: 3A
12V: 5.5A
3VSB: 0.375A

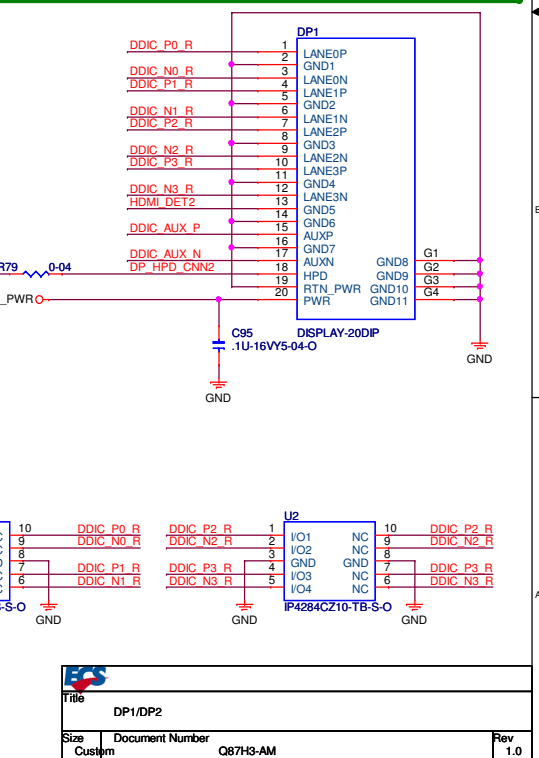
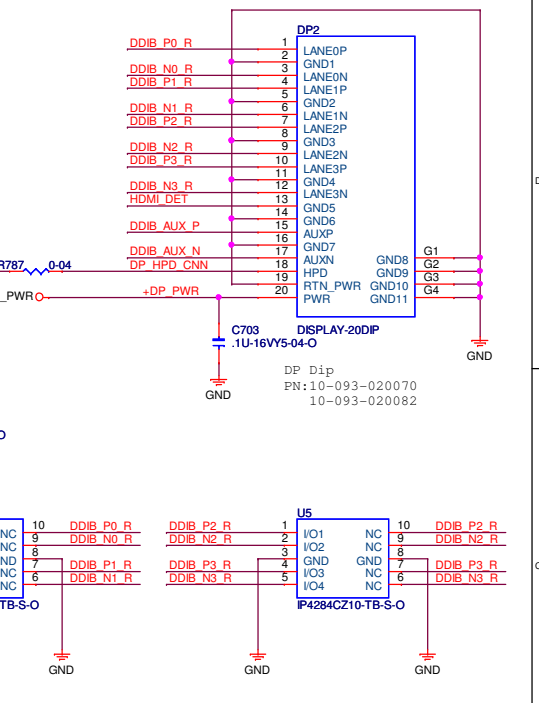
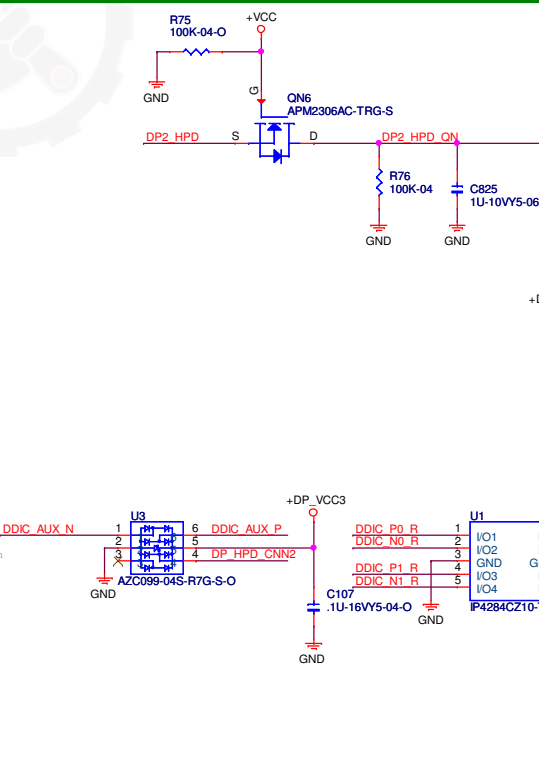
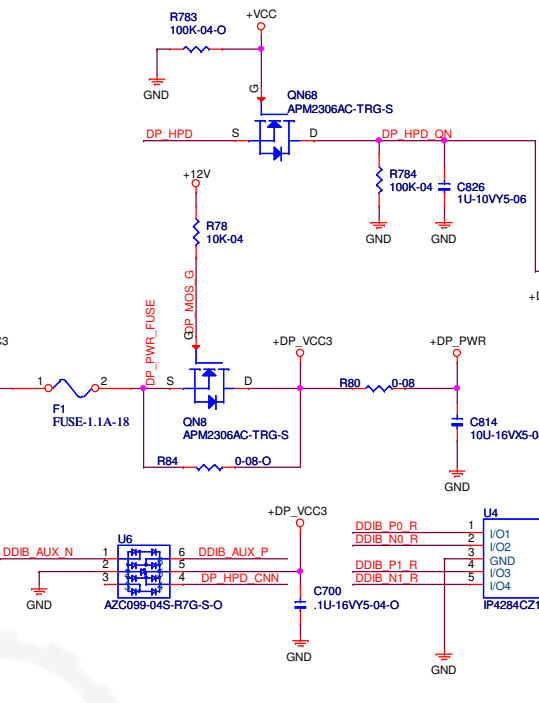
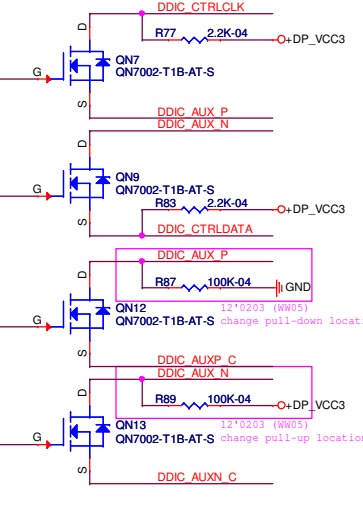
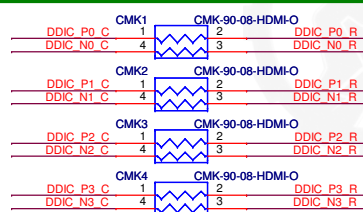
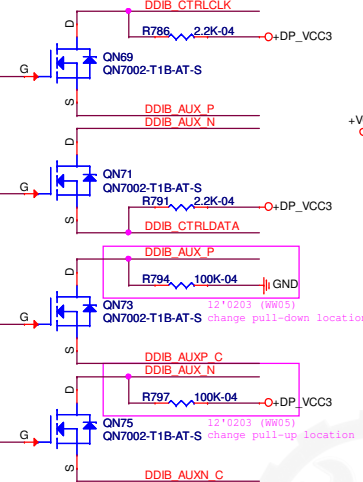
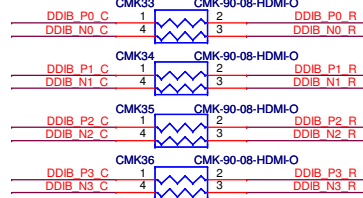
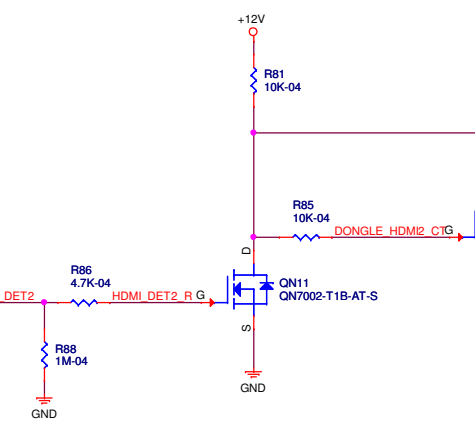
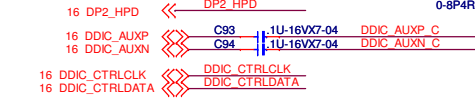
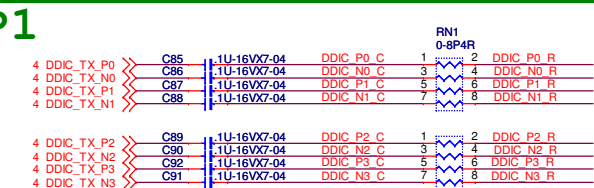
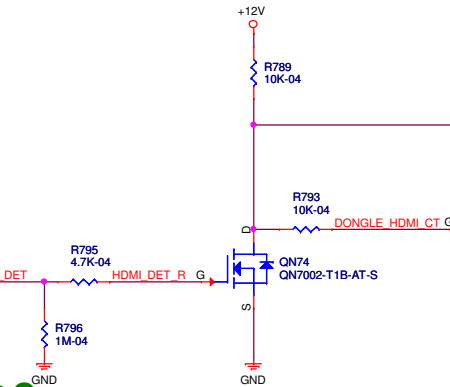
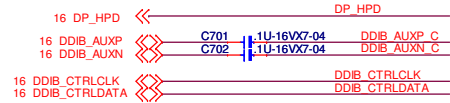
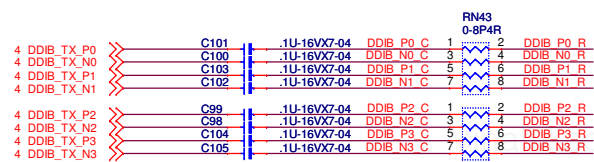


Between PCIe16 & PCIeX1

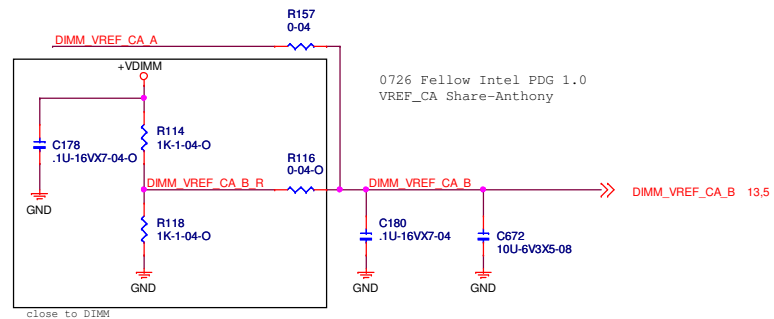
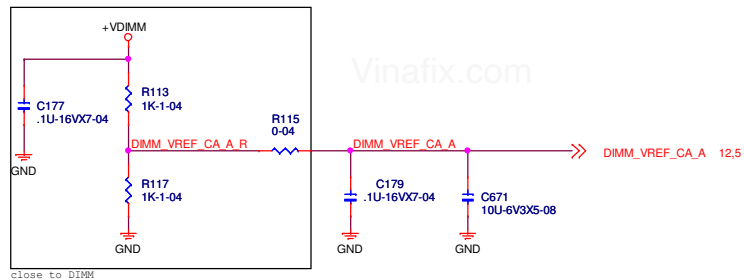


2012/7/05
PCIe Gen3 slot reset circuit update .

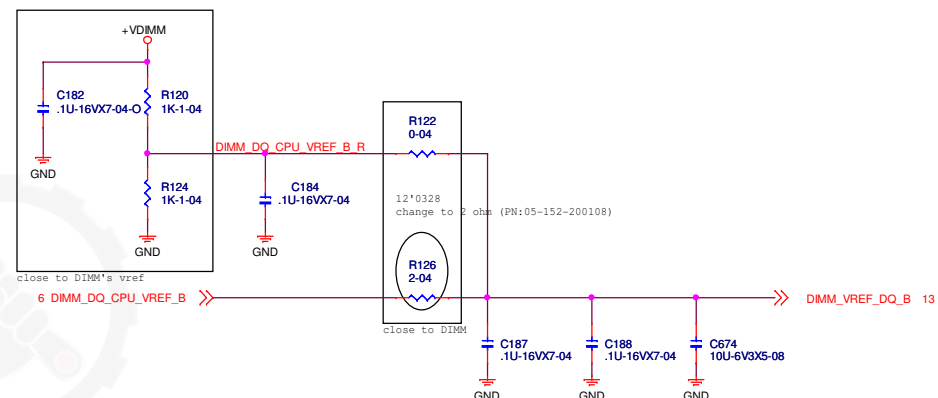
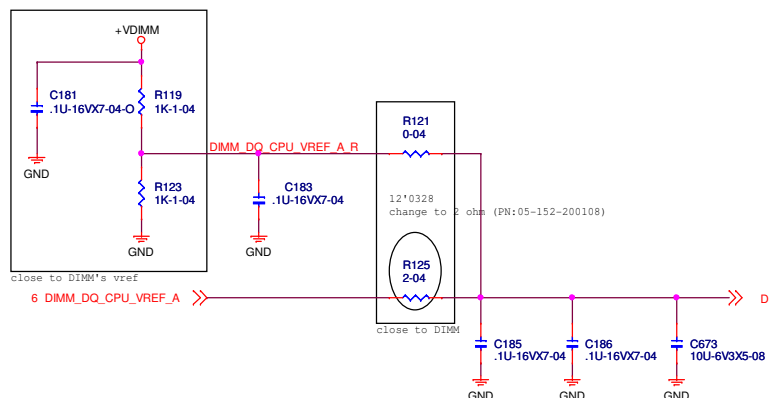
	Ra	Rb	Rc
GPIO PEG Reset	X	V	V
NO GPIO PEG Reset	V	X	X



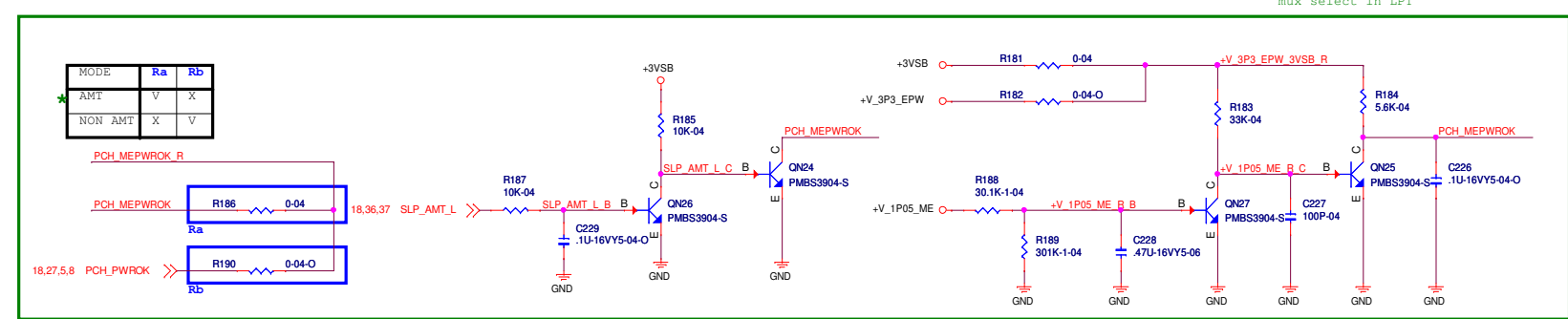
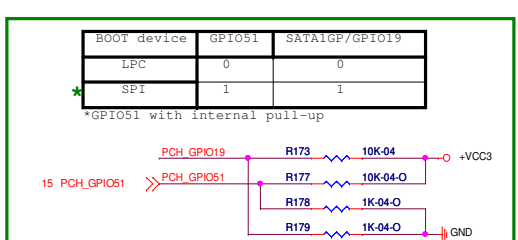
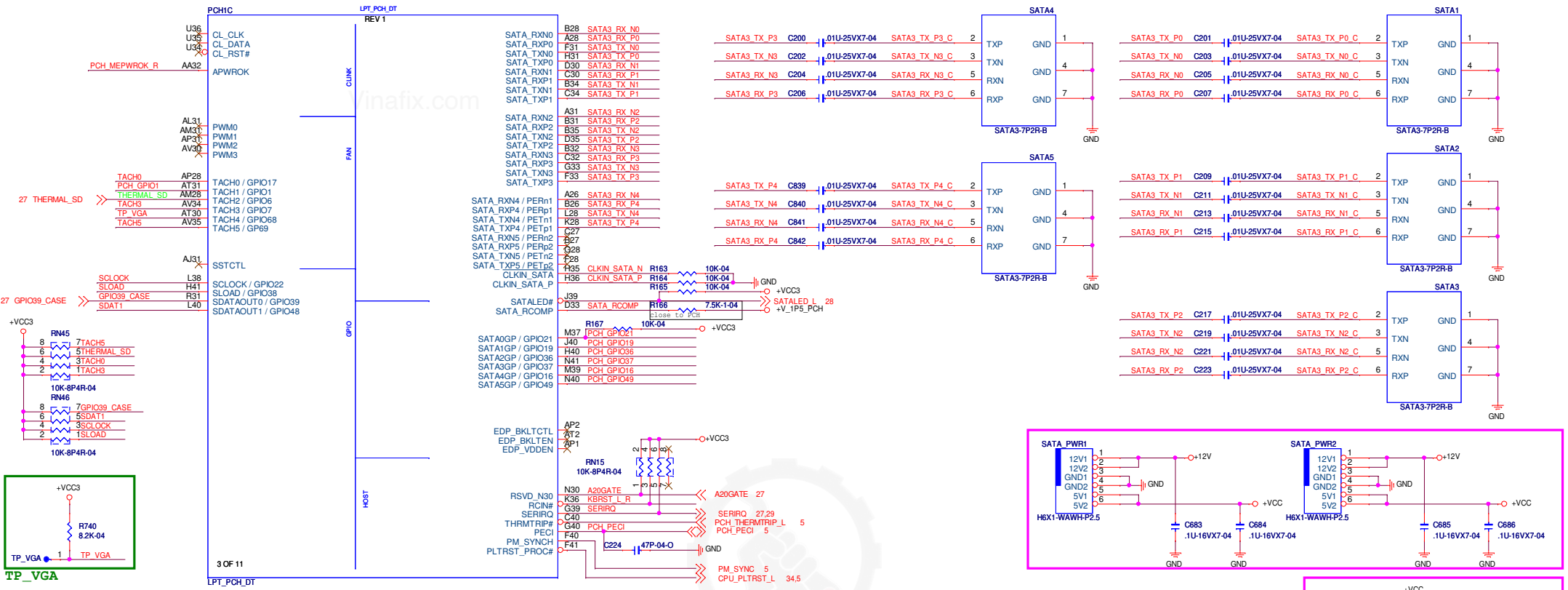




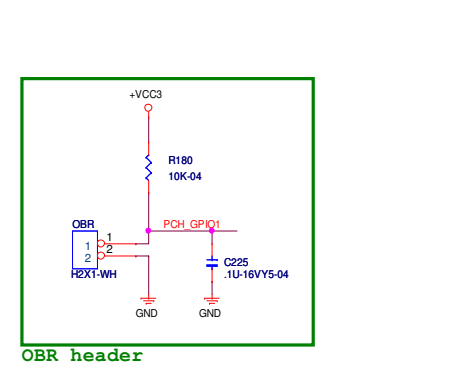
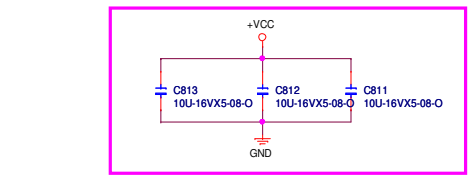
DIMM_VREF_CA Circuit



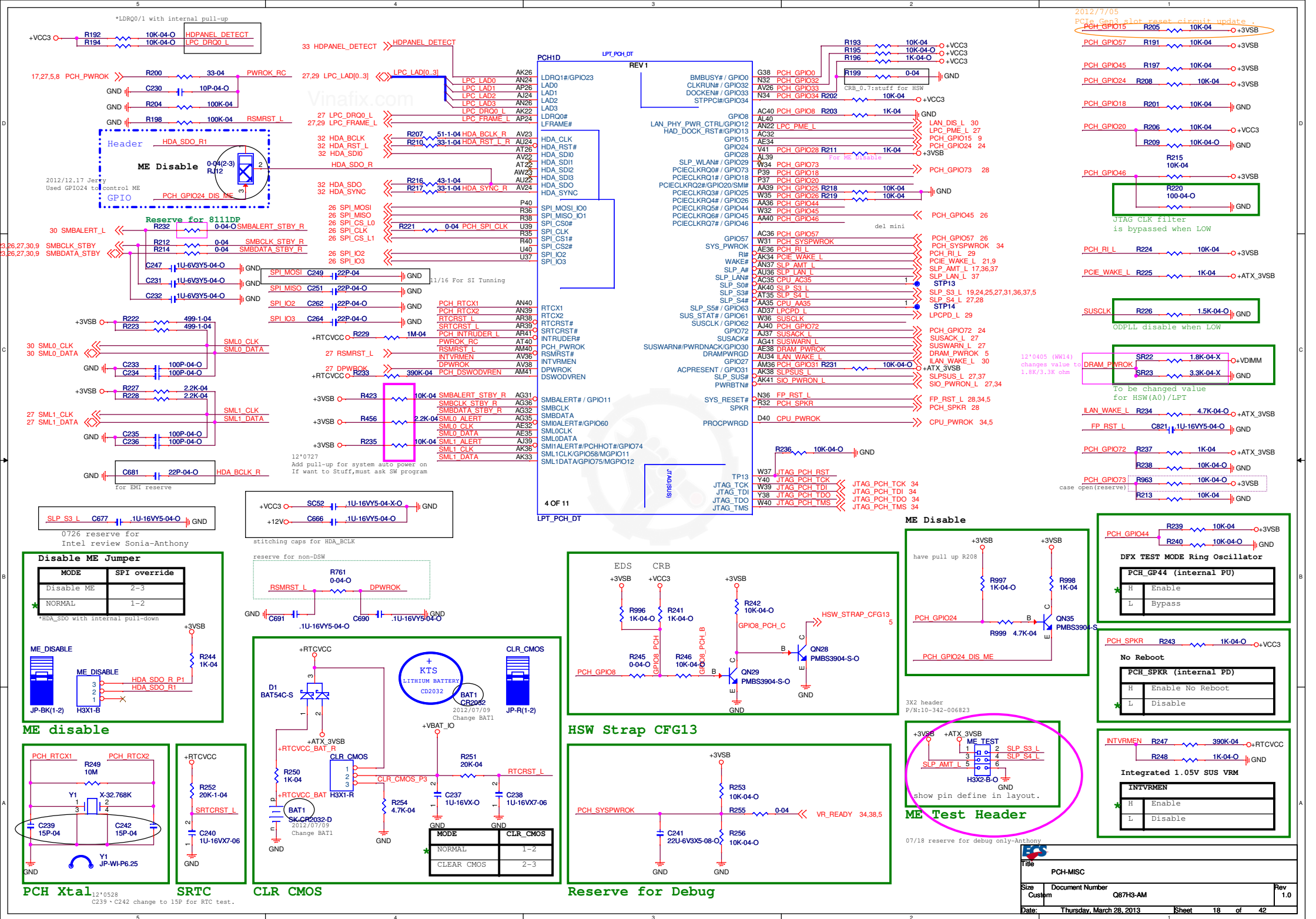
DIMM_VREF_DQ Circuit

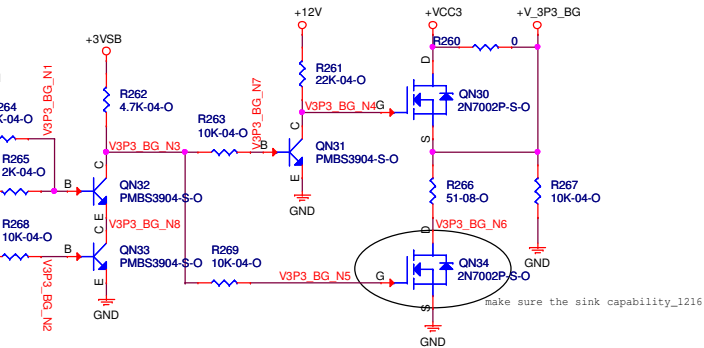


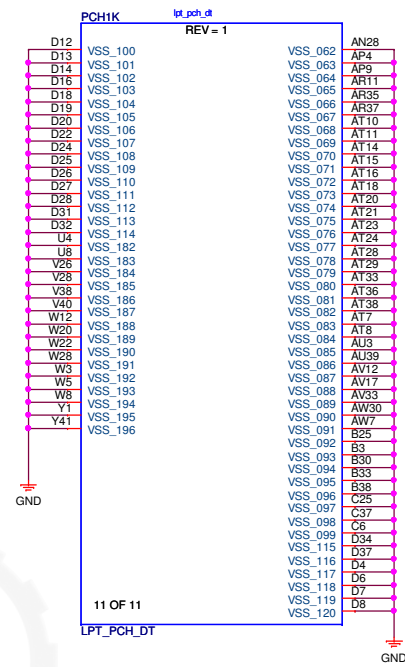
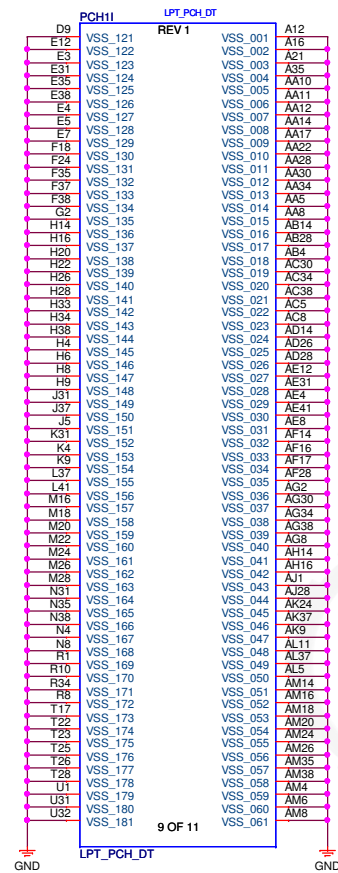
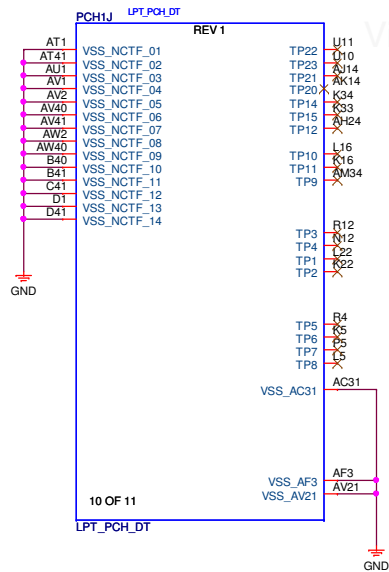
ME PWROK control circuit

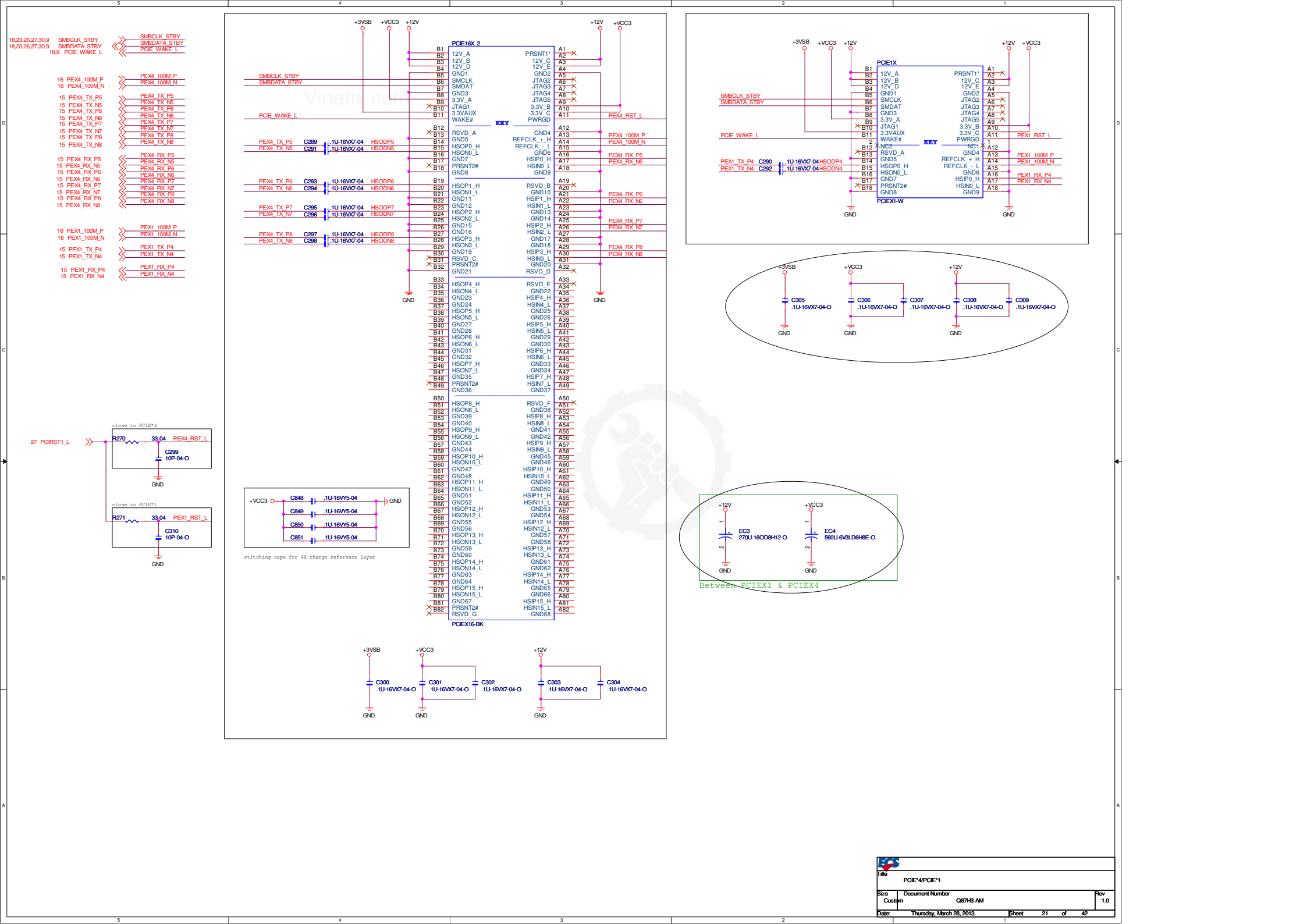


PCH SATA/SATA connector/OBR			
Size	Document Number	Rev	
Custom	Q87H3-AM	1.0	
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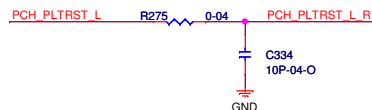








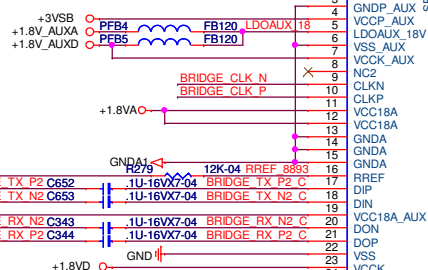
23 AD[31..0] << AD[31..0]
 23 C_BE_L[3..0] << C_BE_L[3..0]
 23 PM66EN << PM66EN
 23 FRAME_L << FRAME_L
 23 IRDY_L << IRDY_L
 23 TRDY_L << TRDY_L
 23 STOP_L << STOP_L
 23 DEVSEL_L << DEVSEL_L
 23 PAR << PAR
 23 SERR_L << SERR_L
 23 PERR_L << PERR_L
 23 LOCK_L << LOCK_L
 23 PCICLK0 << PCICLK0
 23 INTA_L << INTA_L
 23 INTB_L << INTB_L
 23 INTC_L << INTC_L
 23 INTD_L << INTD_L
 23 REQ0_L << REQ0_L
 23 GNT0_L << GNT0_L
 23 PCIRST_L << PCIRST_L



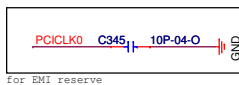
15,27,30 PCH_PLTRST_L << PCH_PLTRST_L

PCH=>

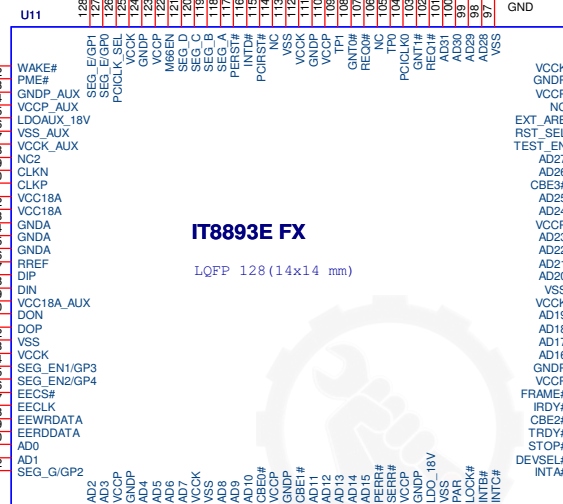
15 BRIDGE_TX_P2 << BRIDGE_TX_P2
 15 BRIDGE_TX_N2 << BRIDGE_TX_N2
 15 BRIDGE_RX_P2 << BRIDGE_RX_P2
 15 BRIDGE_RX_N2 << BRIDGE_RX_N2
 16 BRIDGE_100M_N << BRIDGE_100M_N
 16 BRIDGE_100M_P << BRIDGE_100M_P



BRIDGE_100M_N R280 0-04 BRIDGE_CLK_N
 BRIDGE_100M_P R281 0-04 BRIDGE_CLK_P

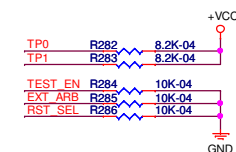
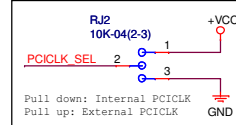
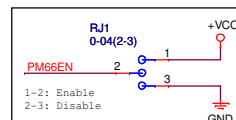
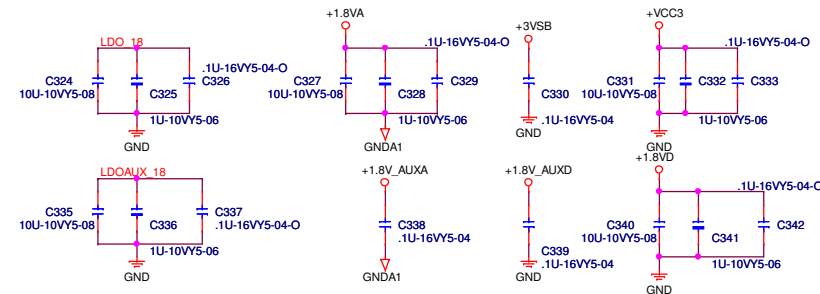


For EMI reserve

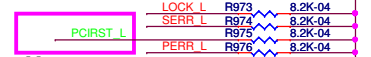
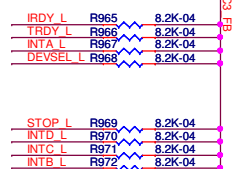


IT8893E FX

LQFP 128(14x14 mm)



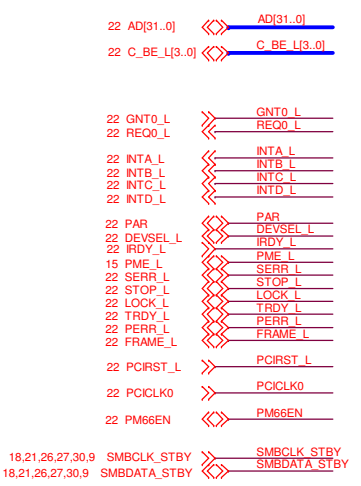
PCI BUS 5V external pull up 2.7Kohm
 PCI BUS 3.3V external pull up 8.2Kohm



0726 Add pull up for ITE review-Anthony

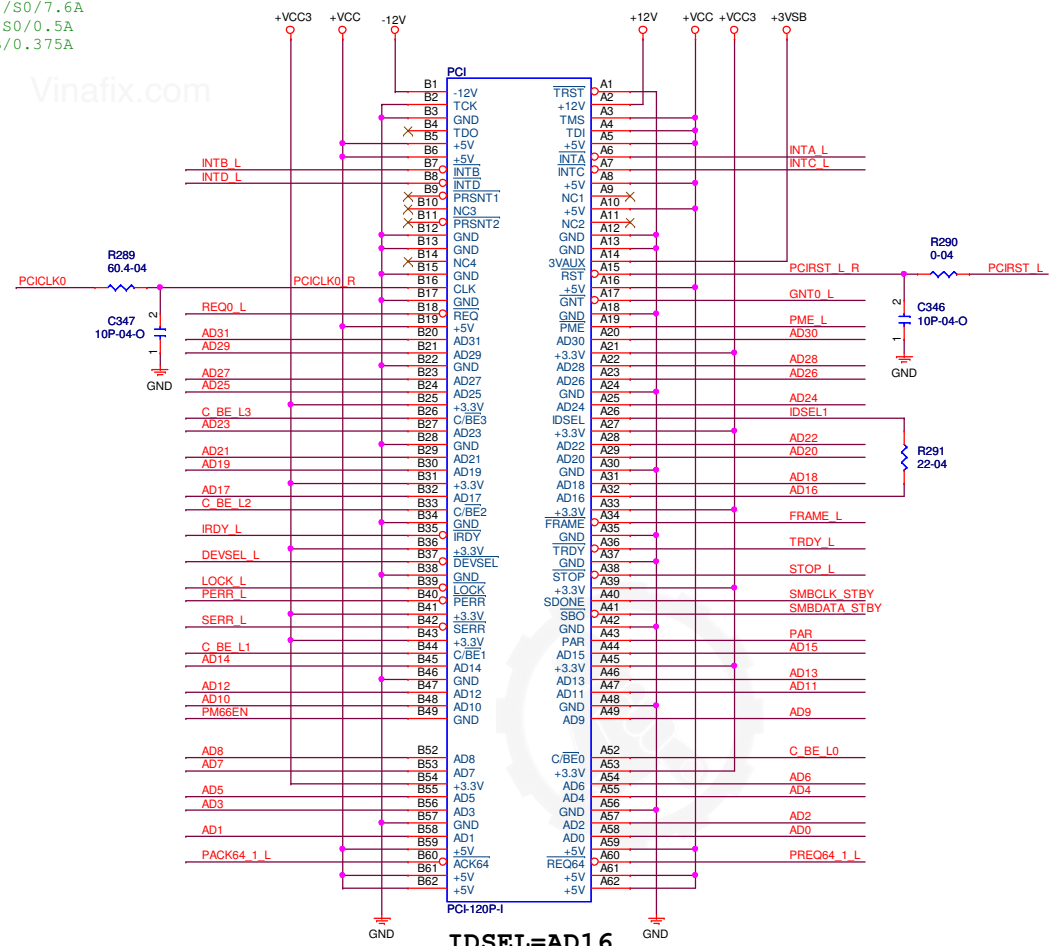
PCIE CLK PCB layout note:
 To meet Differential Impedance :100 ohm +/- 15%
 To meet Single-ended Impedance :50 ohm +/- 15%
 CLKP and CLKN trace width:7 mils
 Space between CLKP and CLKN:14 mils
 L1 & L2 height:5 mils
 The signal traces Number of vias: 4 (Max.)
 The signal trace above analog GND plane
 Spacing from other groups:>25 mils
 Total trace length: 12 inches (Max.)
 The size of R4;R5 is "0402"
 The size of R6;R7 is "0402"

PCIE DIP;DIN;DOP;DON PCB layout note:
 To meet Differential Impedance :85 ohm +/- 15%
 To meet Single-ended Impedance :50 ohm +/- 15%
 PCIE DIP and DIN trace width:9.5 mils
 PCIE DOP and DON trace width:9.5 mils
 Space between DIP/DIN and DOP/DON:14.5 mils
 L1 & L2 height:5 mils
 The signal traces Number of vias: 2 (Max.)
 The signal trace above analog GND plane
 Spacing from other groups:>25 mils
 Total trace length: 12 inches (Max.)
 The size of C24;C25 is "0402"

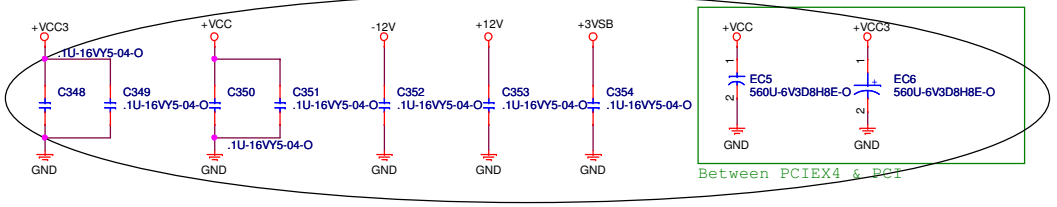


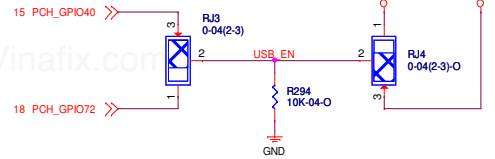
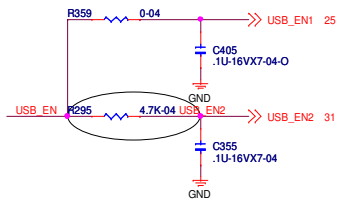
PCI Slot
+VCC/S0/5A
+VCC3/S0/7.6A
+V12/S0/0.5A
+3VSB/0.375A

Vinafix.com

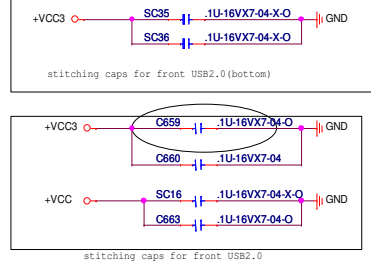


IDSEL=AD16
INT[A, B, C, D]

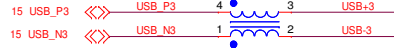




	uP7536 Enable use	RJ?	RJ?	S4/S5 USB_5V_DUAL	Customer
	VDIMM	0ohm (1-2)	NA	0 Volt	Acer S4 w/o S5 w/ USB_5VDUAL
	5VSB	0ohm (2-3)	NA	5 Volt	
*	GPIO	NA	0 ohm	S4 : 0 Volt S5 : 5 Volt	

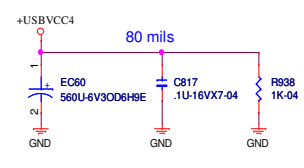
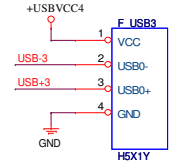
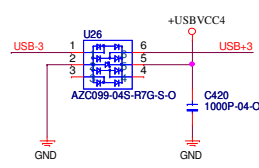
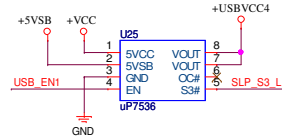


Footprint: CMM21_R0402

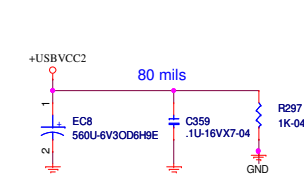
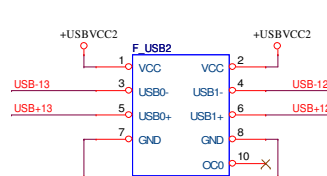
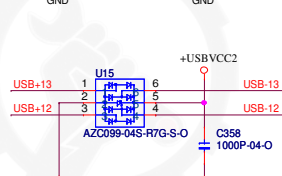
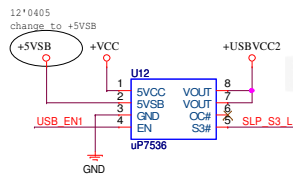
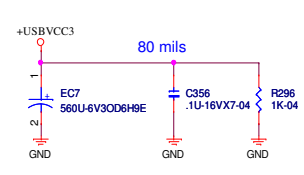
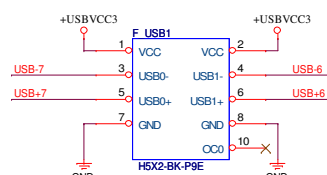
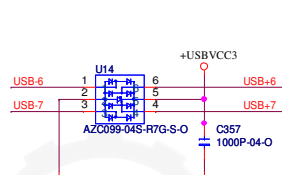
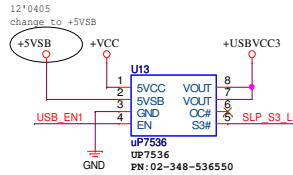


default上電阻, 位置為 CMK37 (1-2), CMK37 (3-4)

V.B 上 Choke

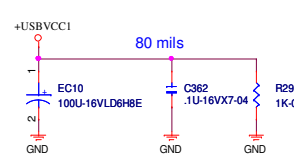
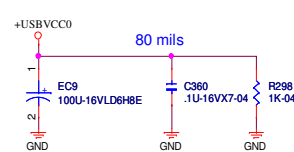
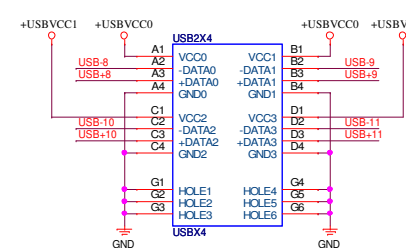
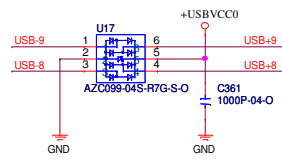
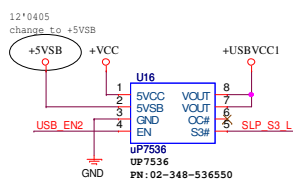
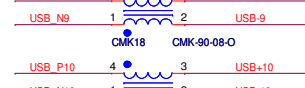
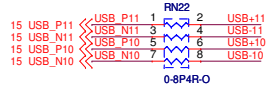
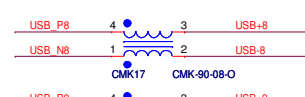
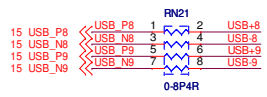


18,19,25,27,31,36,37,5 SLP_S3_L >>> SLP_S3_L

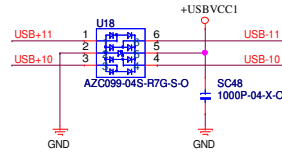


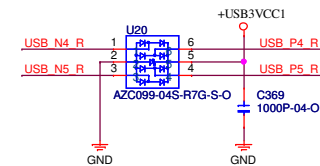
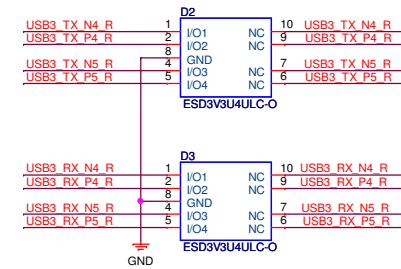
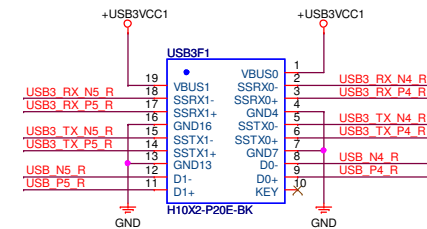
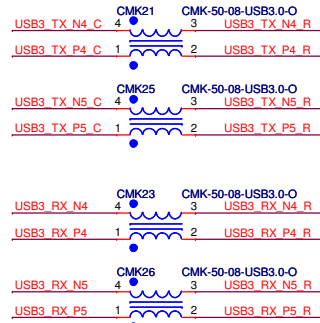
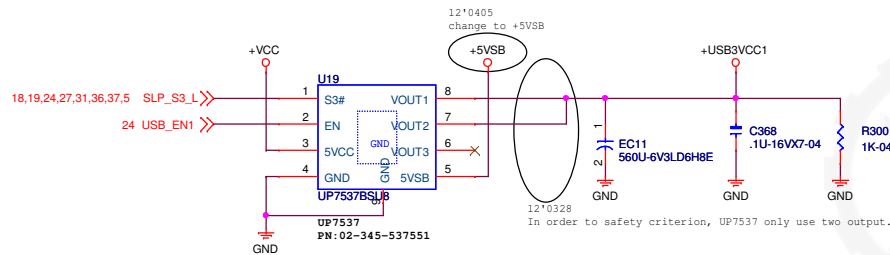
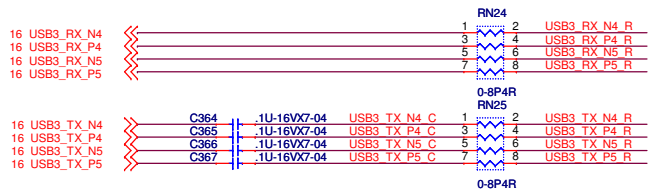
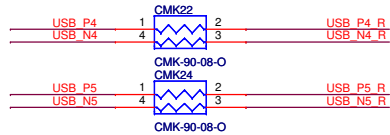
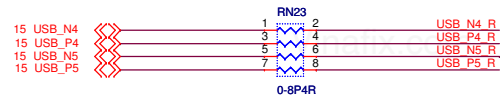
USB2.0 header

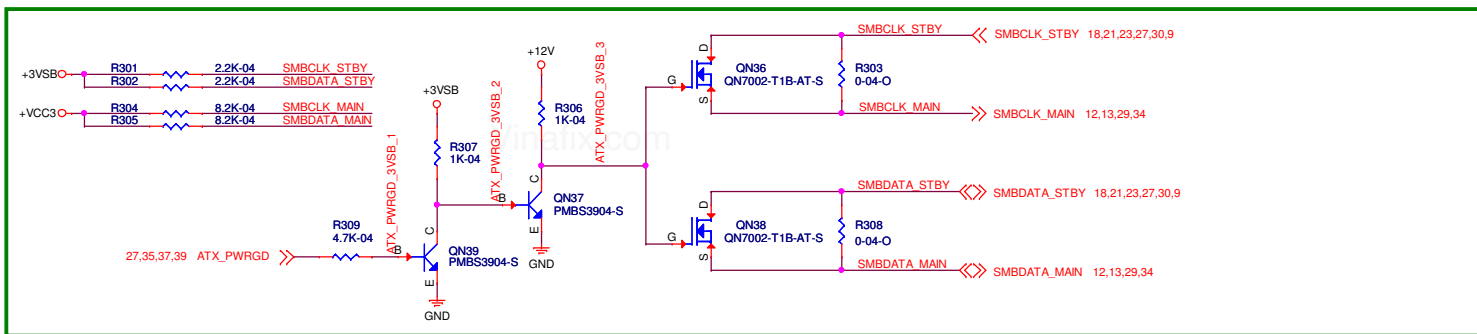
USB2.0 connector



- OC[3:0]# should be connected with USB 2.0 ports 0 - 7 and any 4 of USB 3.0 ports 1 - 6.
- OC[7:4]# should be connected with USB 2.0 ports 8 - 13 and any 4 of USB 3.0 ports 1 - 6.

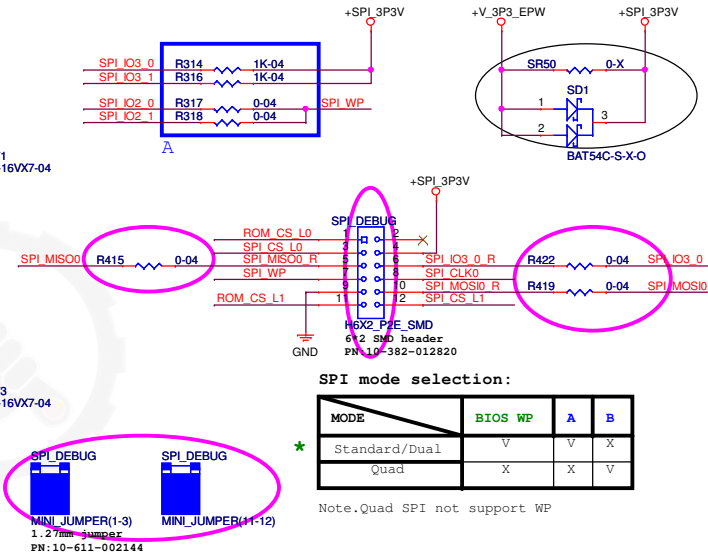
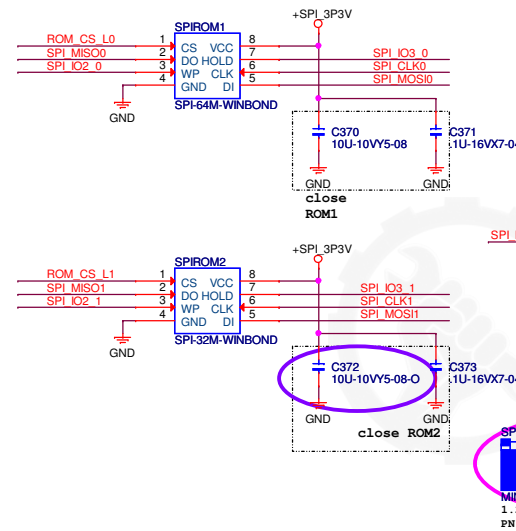
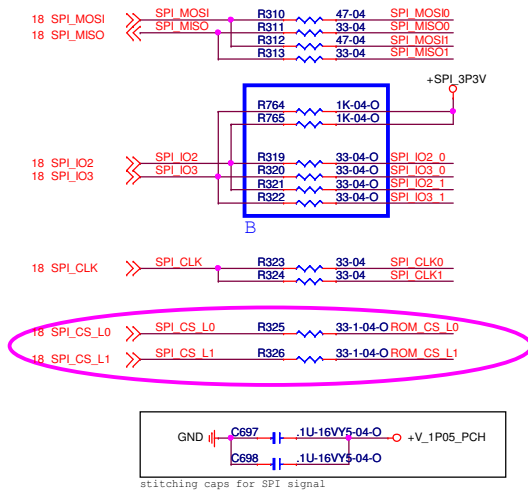






SMBus Logic Circuit

2013'03'20
unstuff S01 change to SR50 for SPI Dubug board



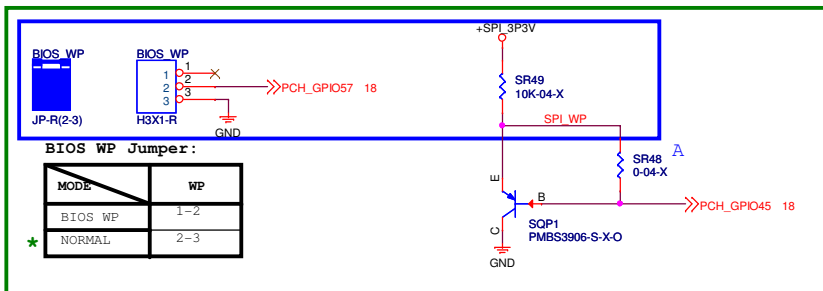
SPI mode selection:

MODE	BIOS WP	A	B
Standard/Dual	V	V	X
Quad	X	X	V

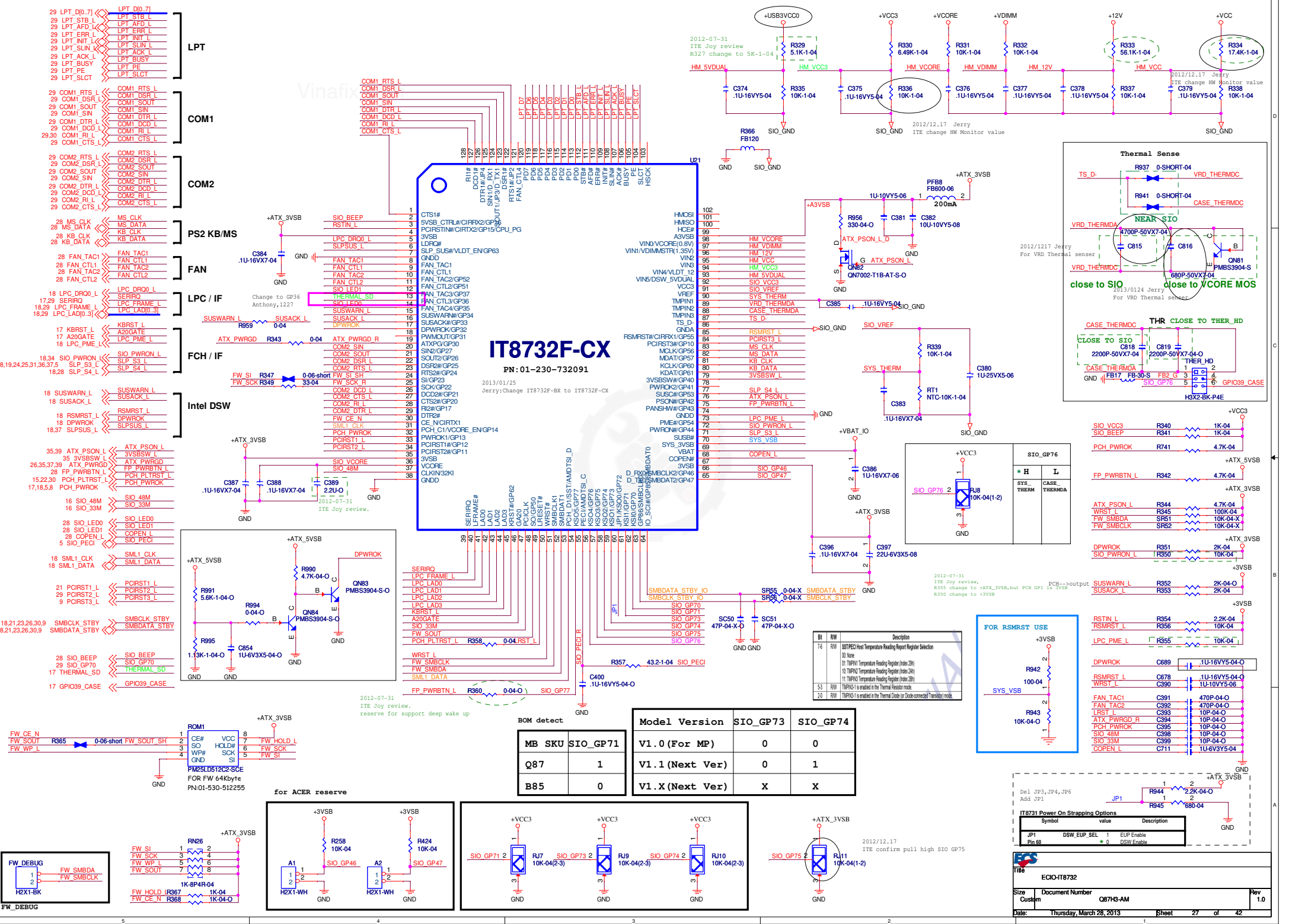
Note: Quad SPI not support WP

07/18 reserve for debug only-Anthony

SPI ROM



BIOS WP

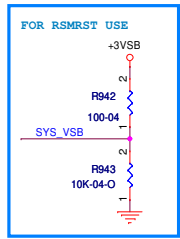


IT8732F-CX

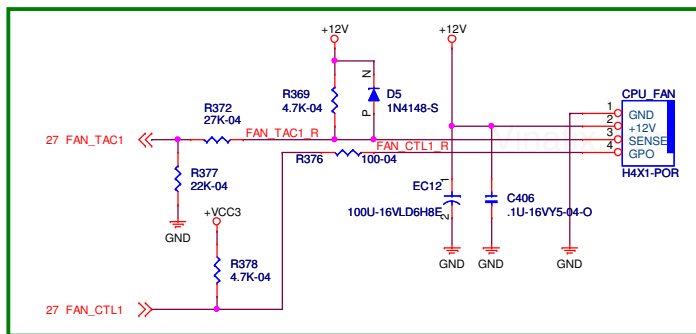
PN: 01-230-732091

2013/01/25 Jerry: Change IT8732F-BX to IT8732F-CX

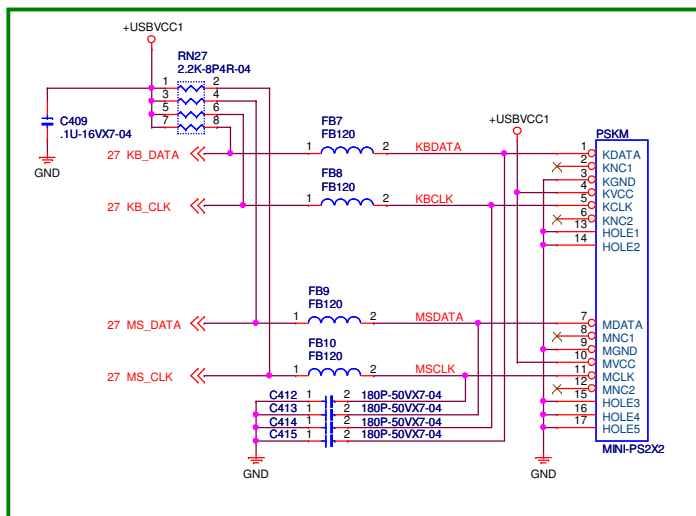
BOM detect		Model Version	SIO_GP73	SIO_GP74
MB SKU	SIO_GP71	V1.0 (For MP)	0	0
Q87	1	V1.1 (Next Ver)	0	1
B85	0	V1.X (Next Ver)	X	X



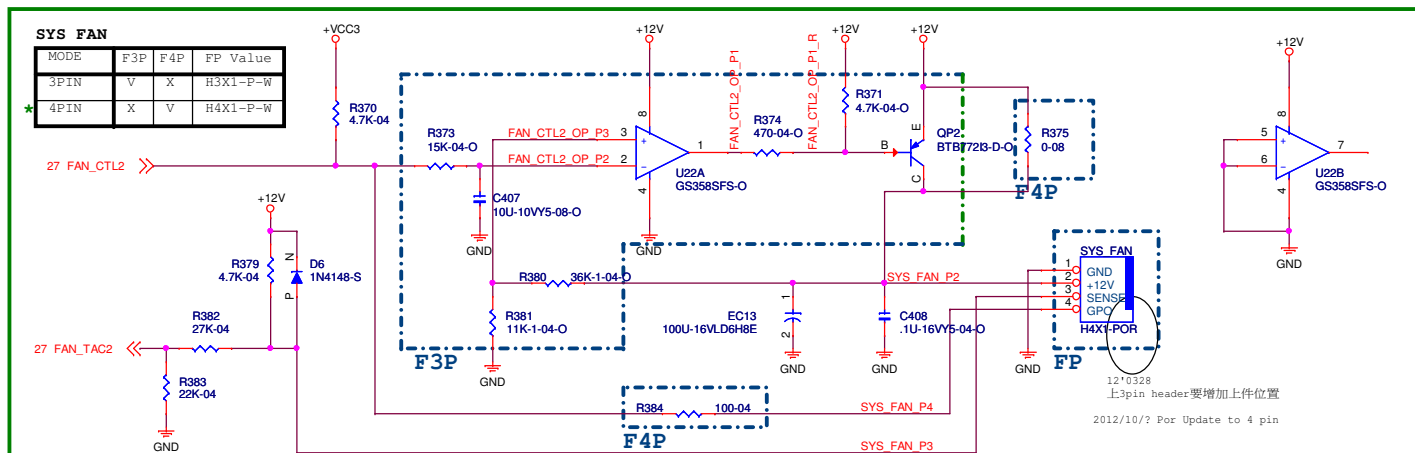
ECO-IT8732		Size	Document Number	Rev
Custom	Q87H3-AM			1.0
Date: Thursday, March 28, 2013		Sheet 27		of 42



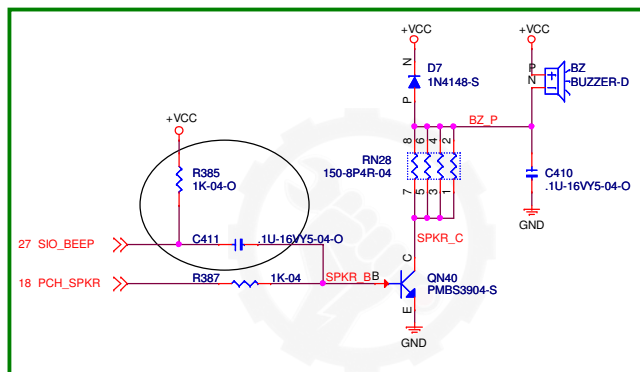
CPU_FAN 4 pin circuit



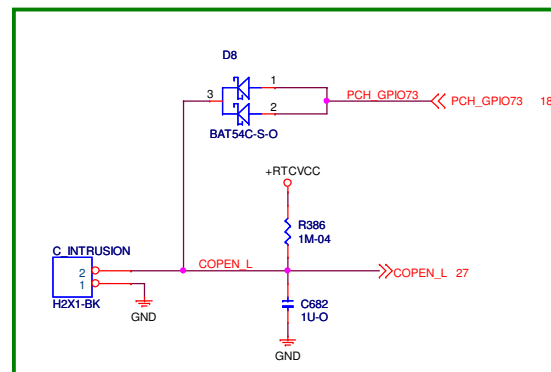
PS2 circuit



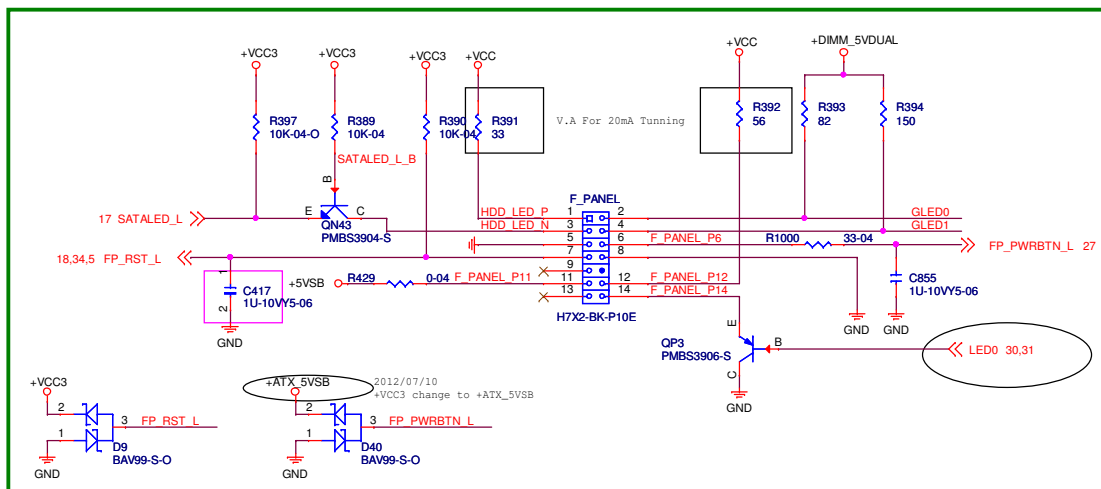
SYS_FAN 3/4 pin co-layout circuit



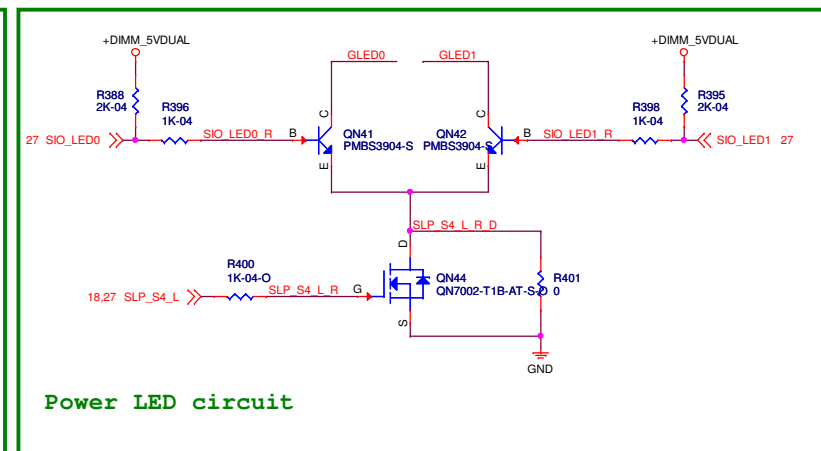
Buzzer circuit



Case open circuit

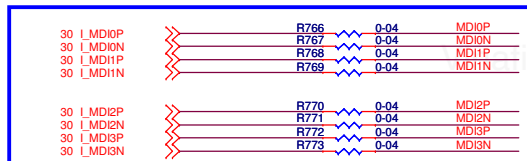


Front Panel circuit

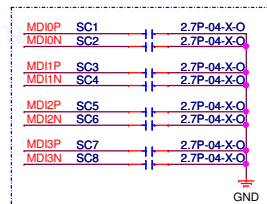
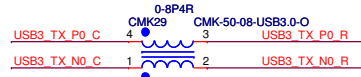
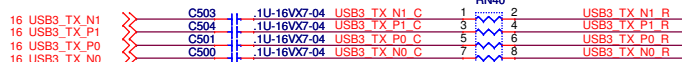
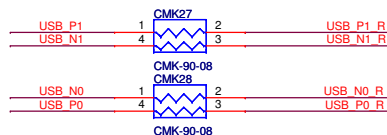
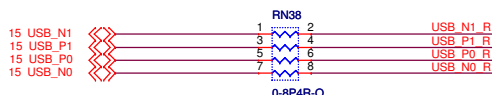
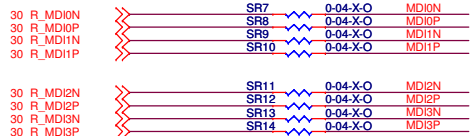


Power LED circuit

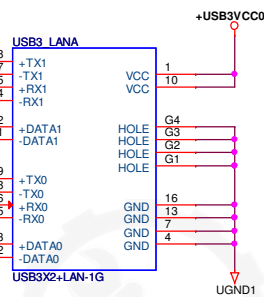
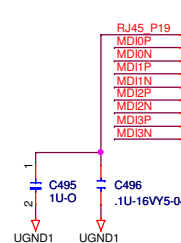
30 LED2
30 LED1
28,30 LED0



Q87

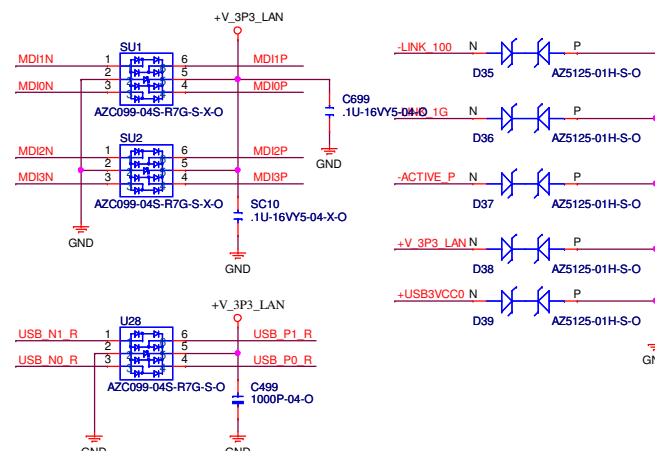


For EMI

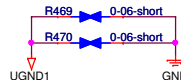
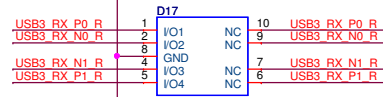
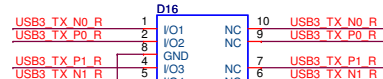
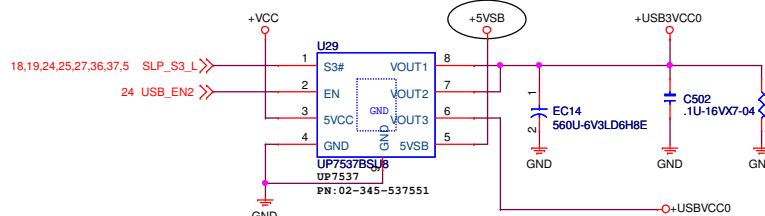


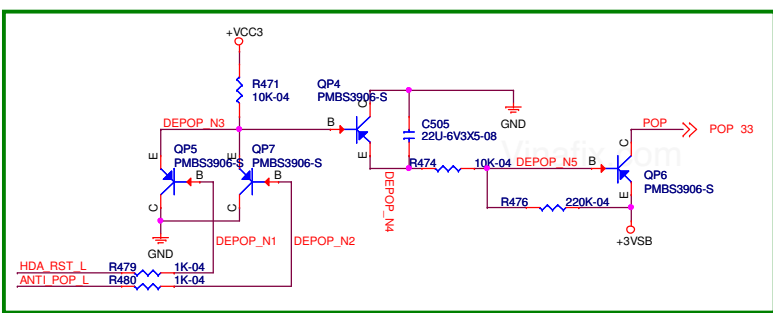
USB3_0+LAN
P/N:10-084-032241

Close to RJ45 Connector



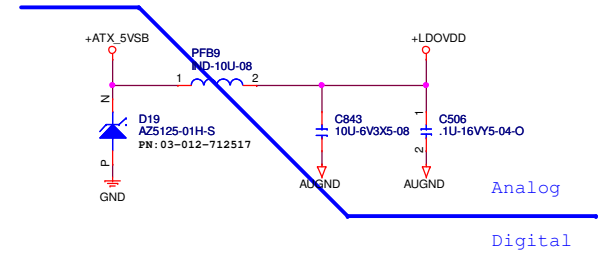
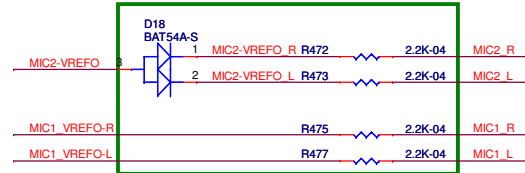
12*0405
change to +5VSB



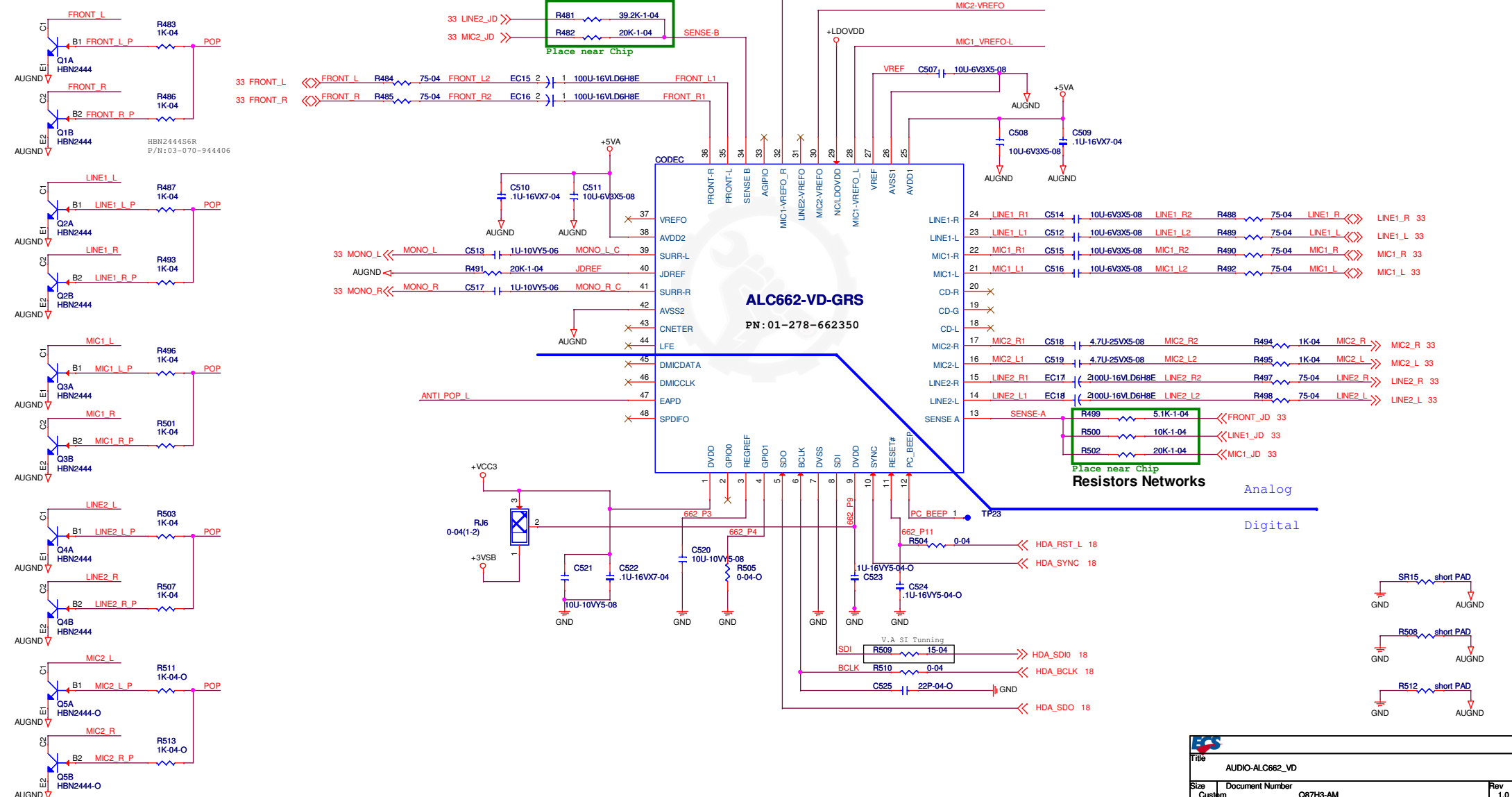


De-pop circuit

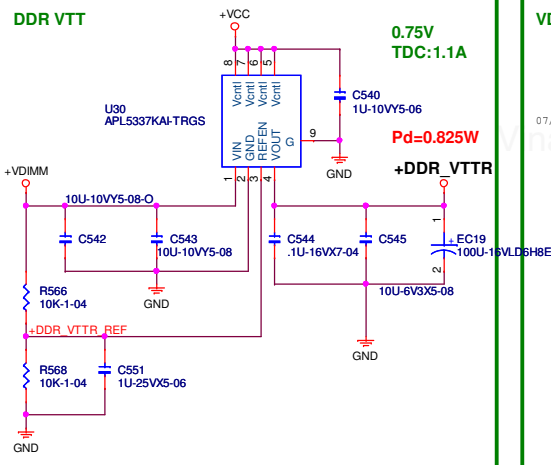
MIC Bias



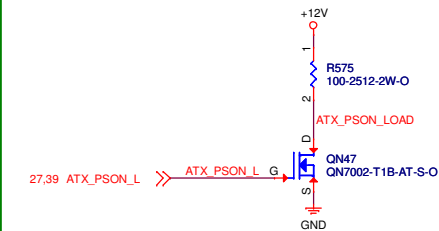
Resistors Networks



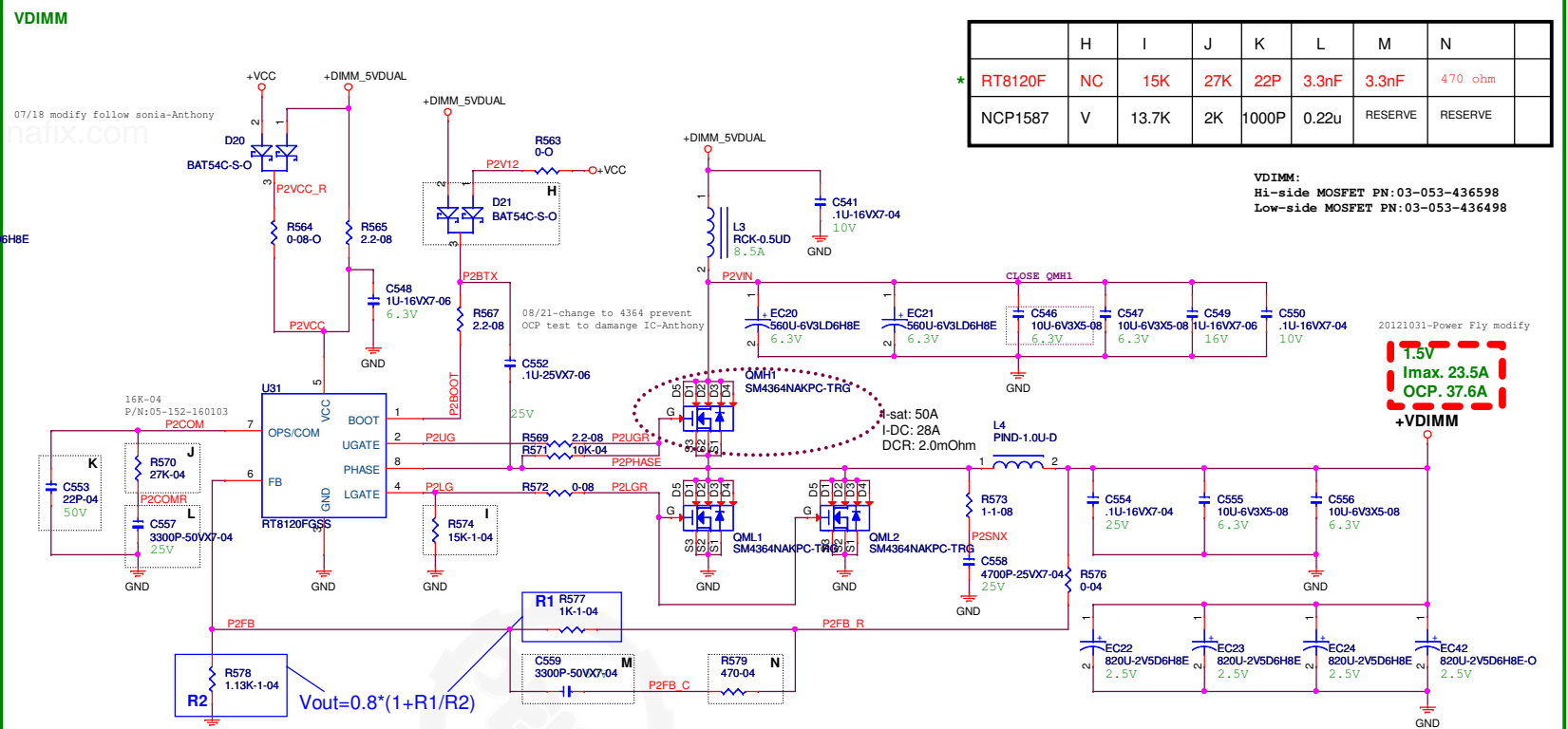
DDR VTT



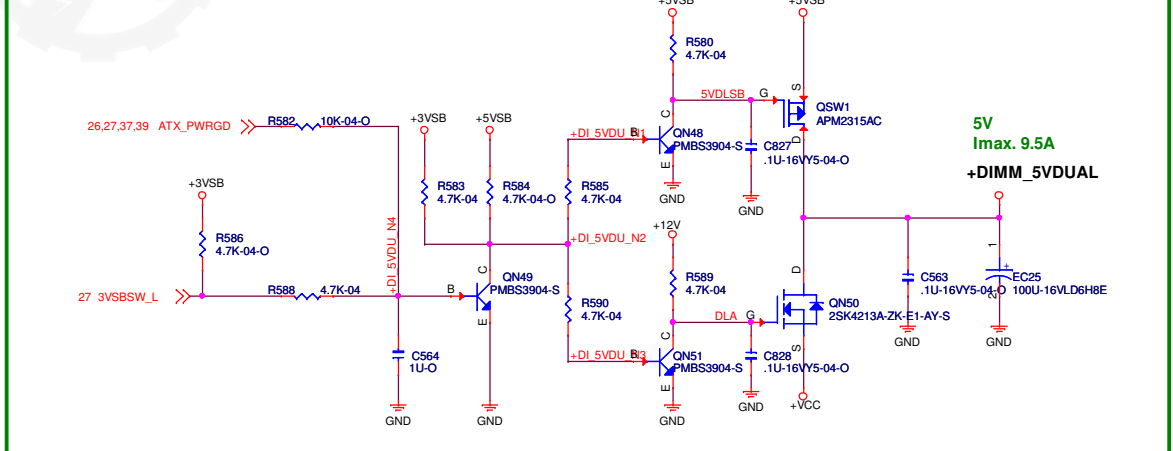
Dummy Load for ATX power



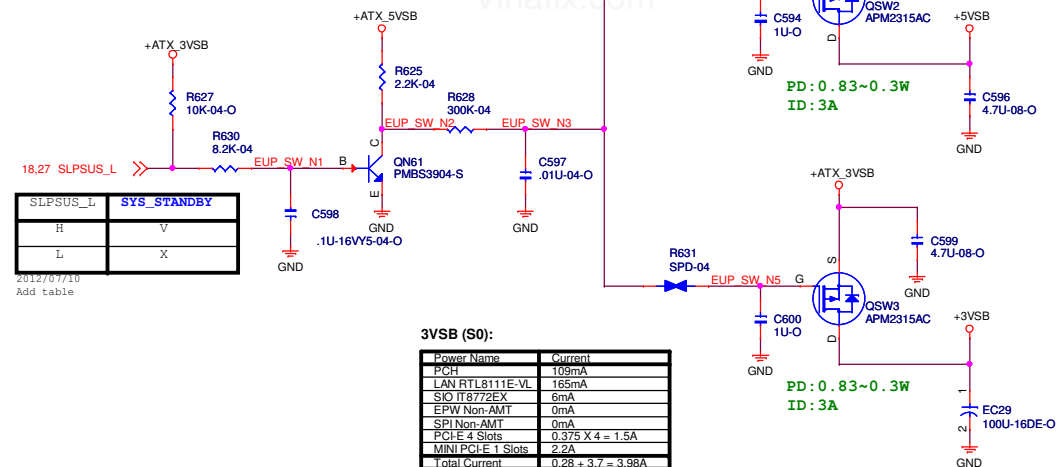
VDIMM



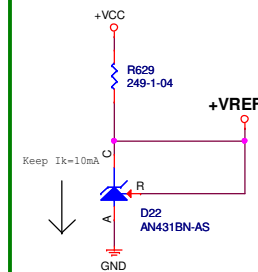
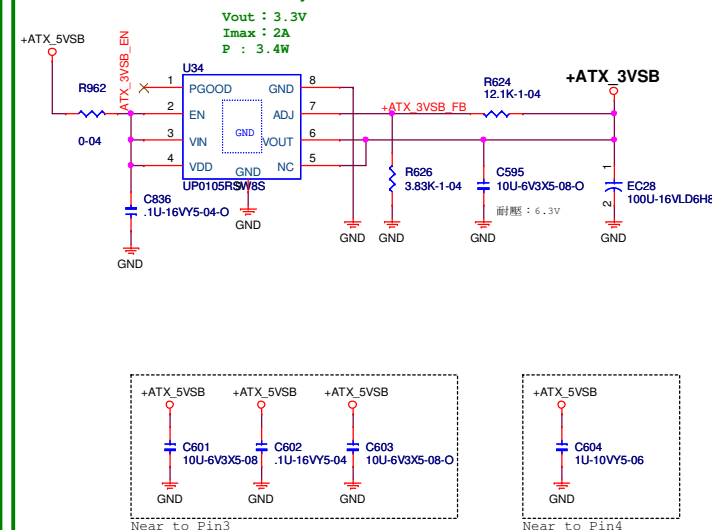
5VDUAL



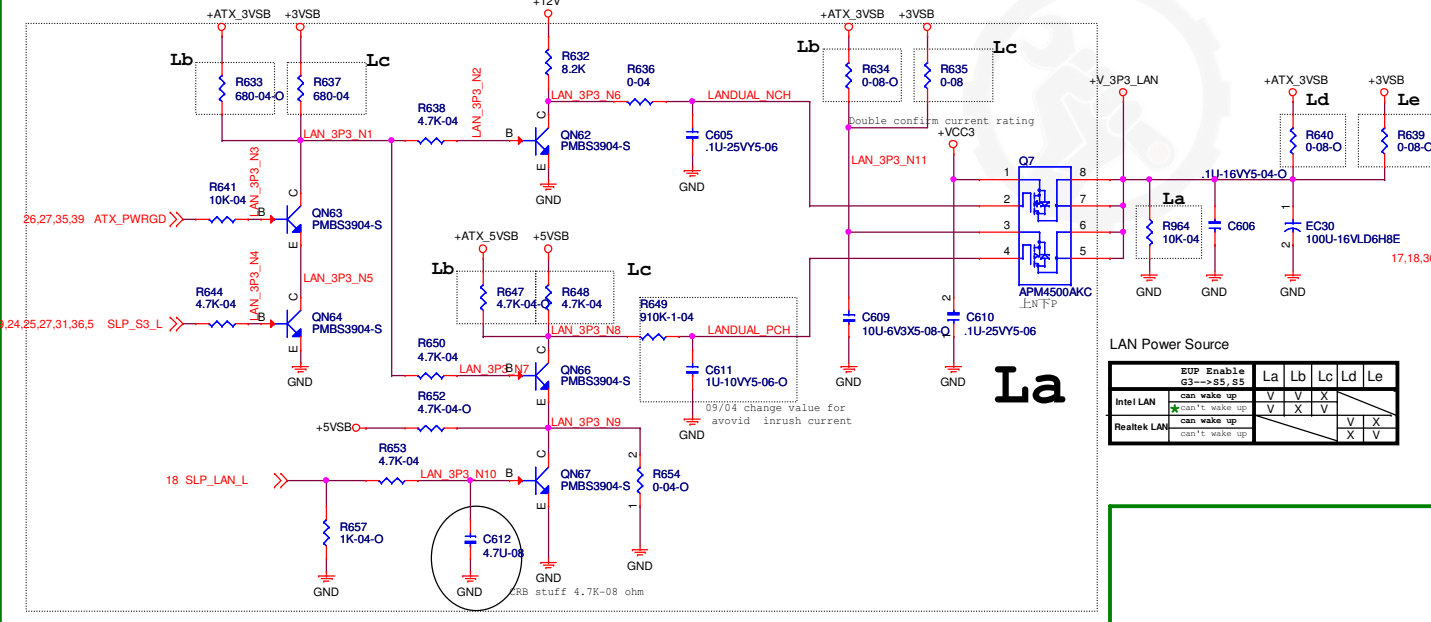
EuP Lot6 Power Saving Circuit



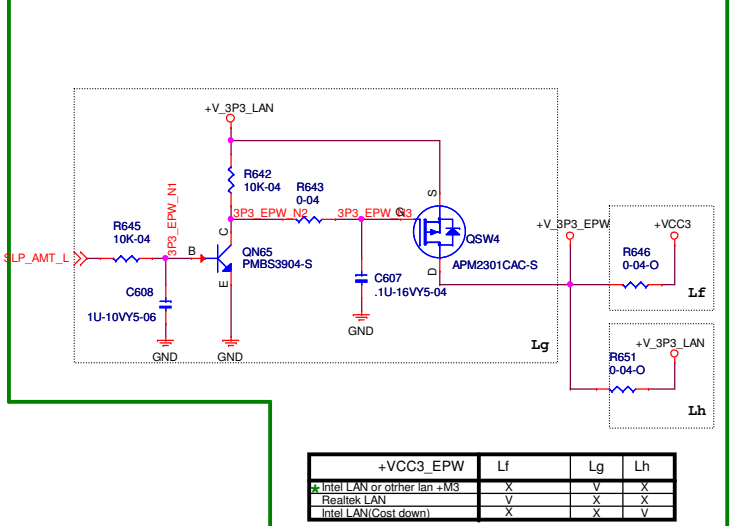
+3V Standby



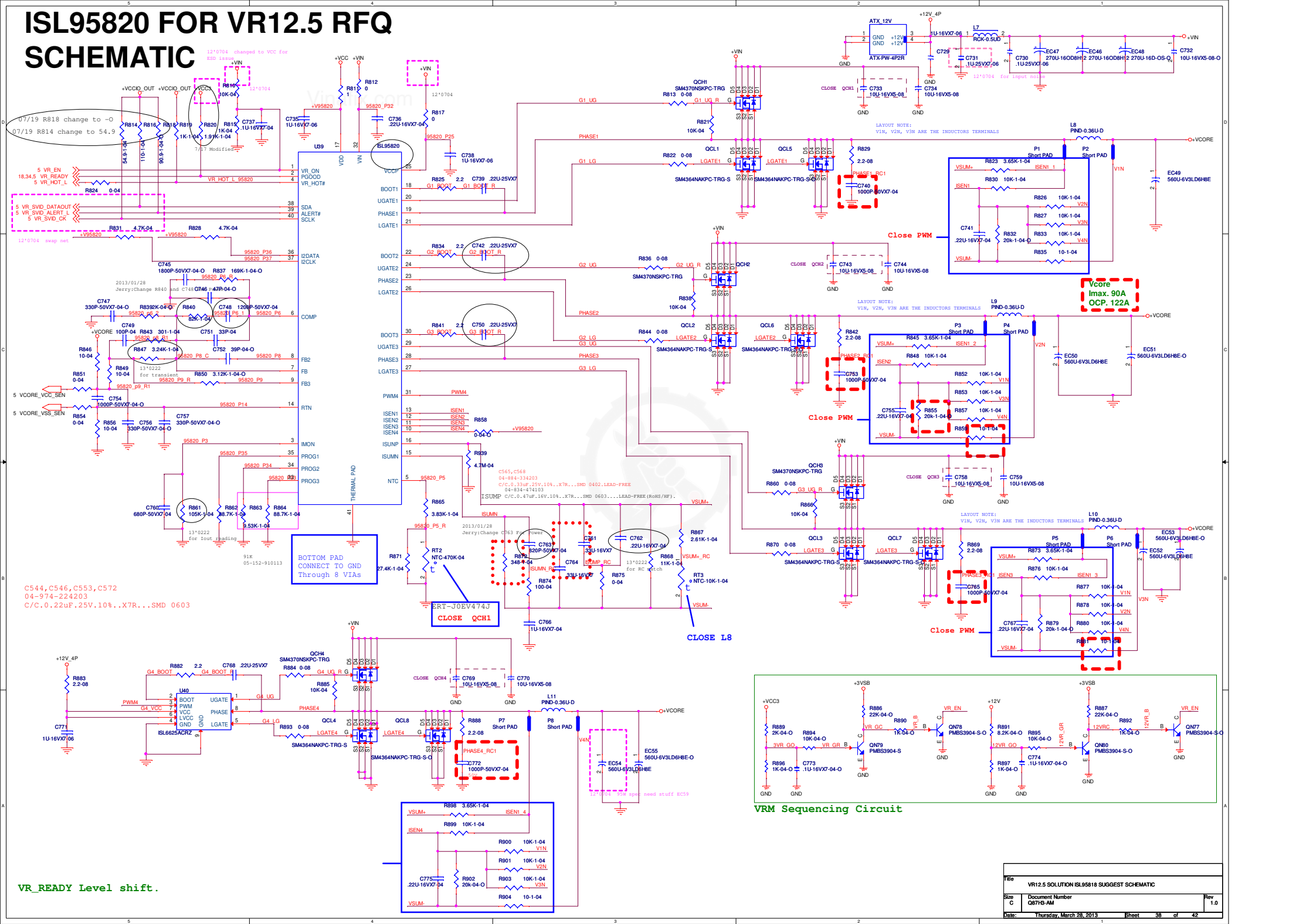
LAN Power Circuit



SPI ROM & PCH Power Circuit



ISL95820 FOR VR12.5 RFQ SCHEMATIC



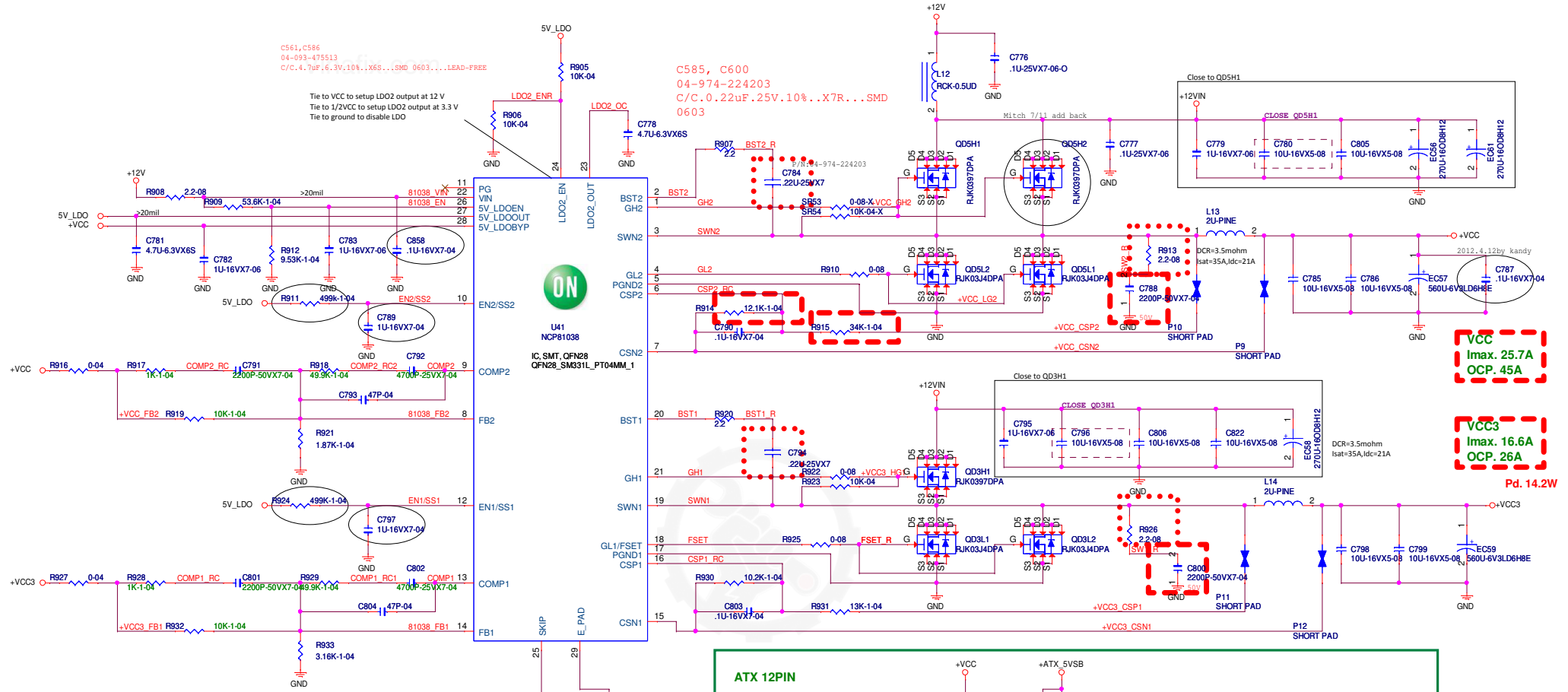
VRM Sequencing Circuit

Title VR12.5 SOLUTION ISL95818 SUGGEST SCHEMATIC			
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C561, C586
04-993-475513
C/C. 4.7uF, 6.3V, 10%, X6S...SMD 0603...LEAD-FREE

Tie to VCC to setup LDO2 output at 12 V
Tie to 1/2VCC to setup LDO2 output at 3.3 V
Tie to ground to disable LDO

C585, C600
04-974-224203
C/C. 0.22uF, 25V, 10%, X7R...SMD 0603



DCM programming pin:

1. Ground this pin to setup automatic CCM/DCM transfer with 33 KHz minimum switching frequency limitation;
2. Connect this pin to VCC to force CCM operation;
3. Leave this pin open to give automatic CCM/DCM transfer with 33 KHz minimum switching frequency for channel 1 but forced CCM for channel 2.

The Rs1, Rs2 and C can be calculated as:

$$C = (R_{S1} // R_{S2}) \cdot \frac{L}{DCR}$$

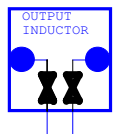
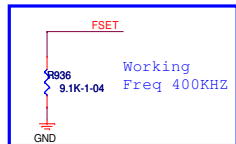
The inductor peak current limit is:

$$I_{LIM(Peak)} = \frac{V_{in_DC}}{k \cdot DCR} \cdot \text{where } k = \frac{R_{S2}}{R_{S1} + R_{S2}}$$

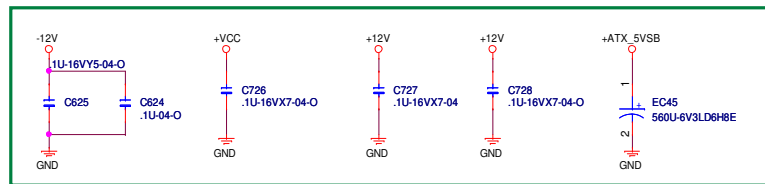
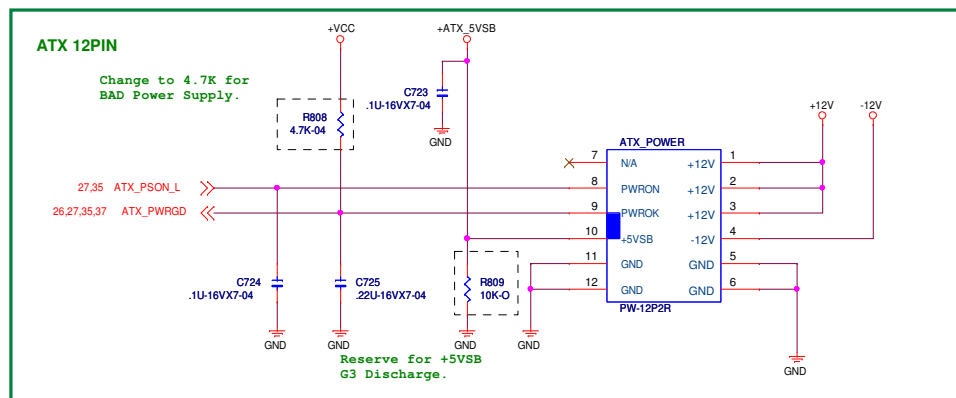
The DC current limit is:

$$I_{LIM} = I_{LIM(Peak)} \cdot \frac{V_o \cdot (V_{in} - V_o)}{2 \cdot V_{in} \cdot f_{SW} \cdot L}$$

SPxx PLACE ON THE
SOLDER SIDE,
CLOSE INDUCTOR



BOTTOM PAD
CONNECT TO
GND Through
5 VIAs



DC/DC VDIMDDR_VTT/5VDUAL			
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